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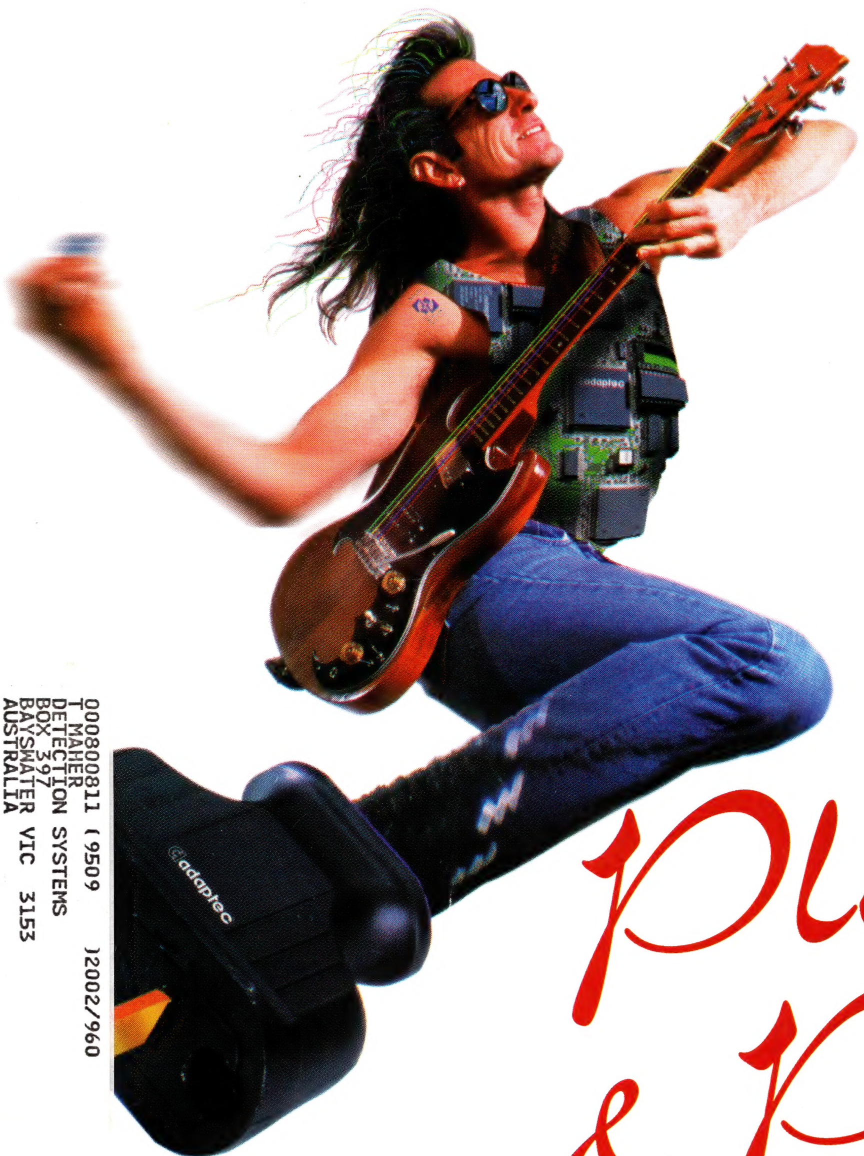
THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

MARCH 2, 1995



Plug & Play

pg 33

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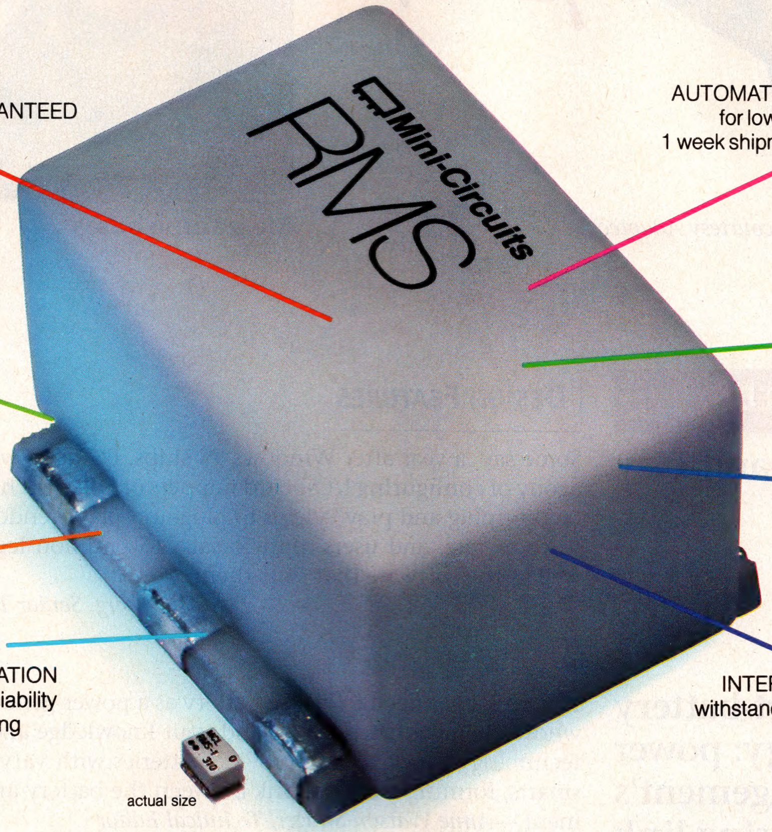

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CIRCLE NO. 97

EDN MARCH 2, 1995

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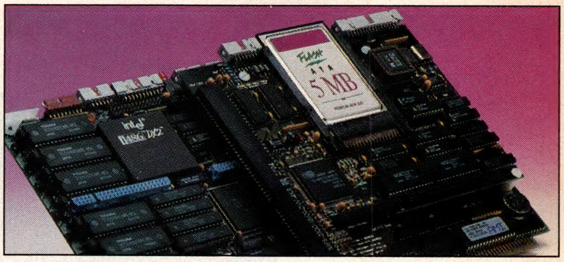
COVER STORY (Photo courtesy Adaptec) 33

Smart-battery technology 47

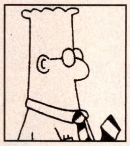


Mezzanine buses 67

EDN

DESIGN FEATURES

OUT IN FRONT



EDN DESIGN IDEAS

EDN COLUMNIST

Don't assume that the software crowd will "come up with something." Because, if it doesn't, your clever design could bankrupt the company.—*Jack Ganssle, Embedded-Systems Contributing Editor*

EDN PRODUCTS

EDN DEPARTMENTS

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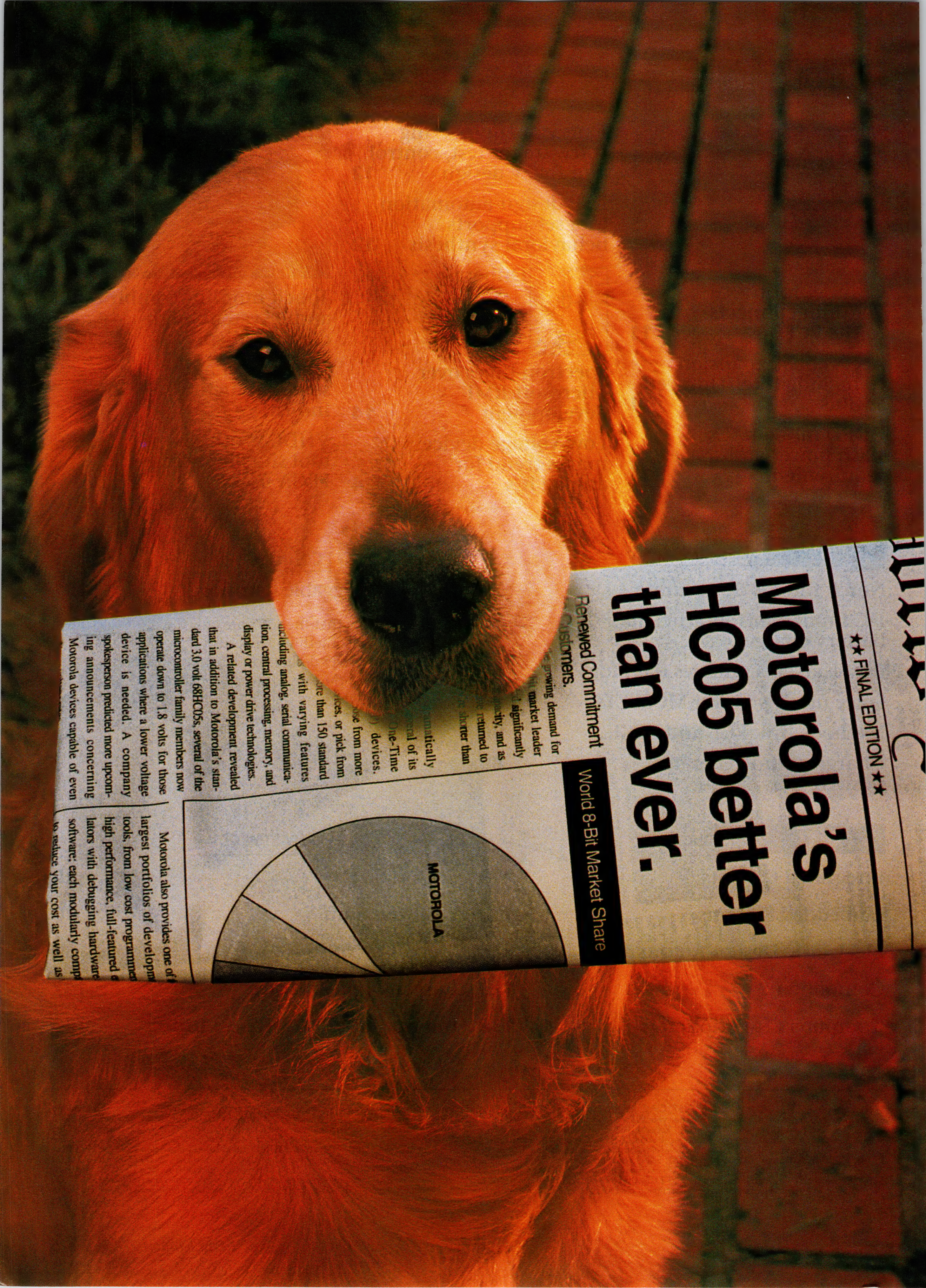
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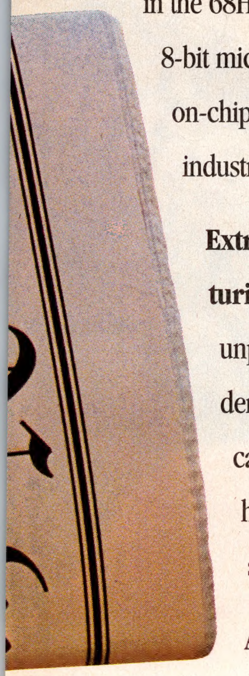

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	Gate Array		Standard Cell			
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Process	0.8 micron CMOS	0.6 micron CMOS	0.8 micron CMOS	0.8 micron CMOS	0.6 micron CMOS	0.6 micron CMOS
Metal	2LM/3LM	2LM/3LM	2LM	2LM	2LM/3LM	2LM
Usable Gate	2LM:4K to 133K 3LM:7K to 232K	2LM:13K to 260K 3LM:22K to 500K	up to 300K	up to 350K	up to 780K	up to 1,110K
Pad Count	80 to 434	104 to 524	up to 444	up to 444	up to 524	up to 524
Number Of Base Array	16	24	–	–	–	–
Operating Voltage	5V	3.3V/5V	3.3V/5V		3.3V/5V	
Gate Delay (Fan out=2)	205V	5V : 130PS 3.3V : 180 PS	190 PS	195 PS	5V : 160 PS 3.3V : 220 PS	5V : 193 PS 3.3V : 266 PS
Toggle Freq.	360 MHz	690 MHz	340 MHz	330 MHz	640 MHz	490 MHz
Power Consumption	3.7μW/gate/MHz	5V:3.6μW/gate/MHz 3.3V:1.3μW/gate/MHz	3.4μW/gate/MHz	1.9μW/gate/MHz	2.7μW/gate/MHz	0.6μW/gate/MHz
Output Drive (mA)	2,4,8 or 12	2,4,8,12 or 24	2,4,8,12 or 24		2,4,8,12 or 24	
ROM Max.bit Size	32K	128K	128K		128K	
RAM Max.bit Size	64K	128K	128K		128K	

*0.5 micron will be available from the 2nd quarter of 1995.

Starting Feb. 1, 1995, Goldstar Electron will be known as LG Semicon.

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CIRCLE NO. 17

CHIP SET FOR THE PENTIUM CONNECTS TO THE PCI BUS

Symphony Laboratories' Rossini, a second-generation chip set, connects the Pentium µP to the Peripheral Component Interconnect (PCI) and ISA buses. The set comprises the SL82C551 cache/memory controller, the SL82C552 data-path controller, and the SL82-C555 system I/O controller. The product supports 50-, 60-, and 66-MHz Pentium-class CPUs from Advanced Micro Devices (AMD), Cyrix, and Intel. Dual voltage references provide 3 or 5V I/O. The device directly drives the PCI and ISA buses, including two fast IDE channels to support four peripherals.

The Rossini chip set from Symphony Labs supports EDO DRAMs and has 3/5V I/O autodetection.

Rossini supports extended-data-out (EDO) DRAMs, which allow improved memory access on motherboards operating as fast as 50 MHz. Burst-EDO DRAMs add a burst counter on the DRAM, permitting access to four levels of data with each address cycle. Four of Rossini's interfaces—the CPU, the DRAM, the SRAM (level-two cache), and the PCI local bus—support dual voltages. The device drives each interface at the correct voltage level, depending on the corresponding V_{CC} pin voltage.

Rossini allows PCI masters to access PCI slaves while the CPU updates main memory. In addition, PCI masters can access main memory while the CPU updates the level-two cache. The combination allows 33-MHz, zero-wait-state burst data transfers. Rossini directly drives Intel's 3.3V, pipelined burst SRAMs, allowing for zero-wait-state performance using a 66-MHz external bus clock.

An intelligent arbiter allows designers to build systems with four PCI slots, an internal master for dual IDE buses, and an ISA bus-master card. You can program the priority of multiple bus masters in a system at several levels to fit design requirements. The device's power-management features include a CPU stop clock, CPU clock throttling, and a system-management mode for AMD, Cyrix, and Intel µPs. Rossini costs $26 in volume quantities.

—by John Gallant

Symphony Laboratories, Santa Clara, CA. (408) 986-1701. **Circle No. 553**

Access.bus expansion to include Intel/Duracell SMBus

The Access.bus Industry Group (ABIG) has announced plans to modify the existing Access.bus specification for one-plug connection of monitors, terminals, mice, and digitizing pads. The new specification will accommodate Intel's System Management Bus (SMBus), which Intel developed jointly with Duracell as a standard interface for smart batteries. The expanded specification will create two-way communications capabilities for both onboard, internal, smart batteries and external Access.bus peripherals. The combined specification will allow users to control system power-management issues as well as external device features. Batteries will now be able to notify users of remaining power and charge requirements and send warnings before failure. Users will be able to prioritize the battery's task list and adjust levels of power consumption through software.

For more information, see our smart-battery article beginning on pg 47.—by Charles H Small

Access.bus Industry Group, Sunnyvale, CA, (408) 991-3517. Circle No. 554

CDPD modem ICs slash power and space requirements

Consumer Microcircuits' FX939 and FX949 dedicated Cellular Digital Packet Data (CDPD) modem ICs drastically reduce power and space requirements over designs that typically use DSP. These modem ICs require less than 8 mA at 3V compared with DSP alternatives that consume up to 100 mA at 5V. Also, the modem's 44-pin TQFP, which suits PCMCIA card designs, requires 0.13 in.² of board space compared with 1.18 in.² for a 132-pin processor alone, ignoring ROM and RAM.

To suit integral cellular-phone/data designs, the FX939 modem IC incorporates three separate functions: a 19.2-kbps full-duplex unformatted Gaussian minimum-shift keying (GMSK) modem; a 10-kbps Advanced Mobile Phone Service (AMPS)-signaling, full-duplex, wide-band data modem; and a full-duplex, 6-kHz AMPS-supervising, audio-tone-signaling decoder and regenerative circuit.

The FX949 targets dedicated radio-modem applications in end-user termi-

(continued on pg 12)

nals. In addition to the 19.2-kbps GMSK modem, this IC includes CDPD frame formatting with Reed-Solomon syndrome and parity generation for error detection. These formatted facilities reduce processing and software overhead on the host processor. Both modem ICs have a 1-mA power-saving mode, operate on 3 to 5.5V supplies, and include parallel and serial data interfaces. The ICs each require three resistors and eight capacitors for a complete design. Price is $20 (1000).

—by Brian Kerridge

***Consumer Microcircuits**, Witham, UK, (44) 1376 513833.*

Circle No. 555

***MXCOM**, Winston-Salem, NC, (919) 744-5050.*

Circle No. 556

Flurry of engineering software for test, control, and fuzzy design

Look for a host of new titles and upgrades of software for designing and simulating control systems, for controlling tests, and for processing and displaying data. The MathWorks is about to announce the Fuzzy Logic Toolbox (from $895), which integrates with MatLab's Technical Computing Environment (TCE) and Simulink graphical simulation environment. According to the vendor, the new toolbox makes MatLab the only product that lets you compare the behavior of systems you design using fuzzy-logic techniques and those you

(continued on pg 14)

DSP DESIGN-AUTOMATION TOOL SET SUPPORTS BEHAVIORAL SYNTHESIS

Version 6.7 of COSSAP, Synopsys's DSP design-automation tool set, includes direct links to the company's Behavioral Compiler and optional DSP developer kits for cosimulation with AT&T and Texas Instruments (TI) DSPs. In addition, the new release of the COSSAP Stream Driven Simulator supports automatic Verilog code generation, giving users their choice of hardware-description languages (HDLs); instantiation of Synopsys DesignWare components for accuracy and predictability through hardware implementation; and links to Synopsys synthesis and VHSIC HDL (VHDL) simulation products.

The COSSAP Stream Driven Simulator employs a dataflow paradigm that enables DSP designers to work completely at the algorithmic level without any architecture or clocking definition, according to Synopsys. The COSSAP HDL Code Generator automatically generates code for Synopsys's Behavioral Compiler, which then performs scheduling, multicycle resource sharing, and other high-level optimizations. This approach takes advantage of the company's DesignWare components and logic-synthesis tools. Using COSSAP, designers can simulate DSP systems up to 10 times faster than they can with other simulators, and, using the Behavioral Compiler, they can implement the hardware for these designs up to 10 times faster, according to Synopsys.

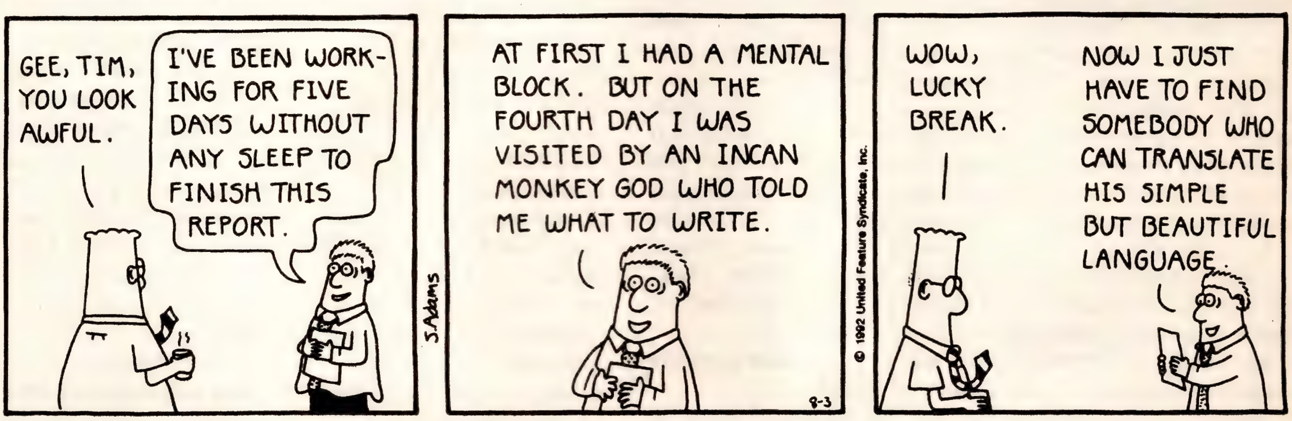
For hardware cosimulation, the COSSAP VHDL simulator interface now supports the Synopsys VHDL System Simulator (VSS). This capability lets designers use VSS's three simulation engines, which support the stages of hardware development. For DSP software developers, Synopsys is working with DSP manufacturers to deliver cosimulation between the COSSAP Stream Driven Simulator and DSP instruction-set simulators. The developer kits for the AT&T DSP1610 and TI TMS320C5x DSPs let designers verify their DSP assembly code in the context of the original system model.

The COSSAP Stream Driven Simulator runs on Synopsys's standard workstation platforms; prices start at $29,000. The COSSAP HDL Code Generator with support for behavioral and register-transfer-level code generation sells for $7500, and COSSAP DSP developer kits cost $7500 each.—by Fran Granville

Synopsys Inc, Mountain View, CA, (415) 962-5000.

Circle No. 557

DILBERT® by Scott Adams



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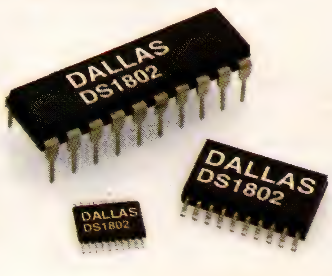

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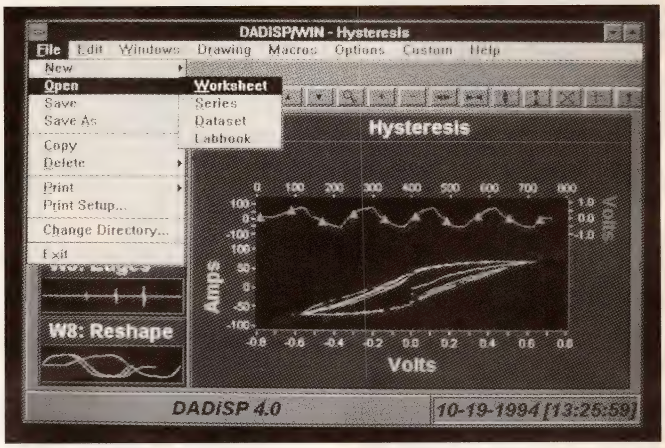
CIRCLE NO. 48

design using classical control theory. The toolbox includes editors for fuzzy interfaces, membership functions, and rules, as well as inference and surface viewers. Supported algorithms include adaptive neuro-fuzzy inference systems and Sugeno-style inferencing systems.

Last month, Hewlett-Packard announced a pair of packages, the first of which, HP Basic for Windows, it developed in cooperation with TransEra Corp. TransEra publishes HT Basic, an MS-DOS-based product that is compatible with HP's workstation-based HP Basic. The new package can run existing HP Basic and HT Basic programs. It costs $950 and runs on Windows PCs without the special coprocessor board that some earlier PC-based HP Basic products required. Registered users of earlier versions of HP Basic can get a $200 credit.

HP's second offering is V3.0 of HP VEE, the graphical programming system for both Windows PCs and Unix workstations. Additions to the new release include a host of widgets, icons, and dialog-box formats that make controlling instruments more straightforward. Although you need a mouse to create VEE applications, the applications can run solely under keyboard control. HP has also revamped VEE pricing. The Windows version now costs $995; Unix versions cost $2995. Run-time-only systems cost $249 for Windows and $495 for Unix. According to HP, the enhancements in HP VEE V3.0 should soon also be available in DT VEE from Data Translation. DT VEE supports the vendor's data-acquisition boards.

DSP Development Corp has announced DaDiSP V4.0 for Windows and Unix. This release of the graphical spreadsheet package conforms to Windows and Open Software Foundation Motif operator-interface standards. The new release marks the introduction of Series Pro-



DaDiSP V4.0's user interface now conforms to Windows guidelines and features the built-in Series Programming Language.

gramming Language (SPL), a complete programming language modeled on C. SPL permits user-defined functions, looping, iteration, conditional branching, array references, and array variables. SPL can also link formulas to "hot" variables containing real or complex numbers, integers, strings, matrices, or data series. Prices for the Windows version of DaDiSP begin at $1895.

—by Dan Strassberg

Data Translation Inc, Marlborough, MA. (508) 481-3700. **Circle No. 558**

DSP Development Corp, Cambridge, MA. (617) 577-1133. **Circle No. 559**

Hewlett-Packard Co, Santa Clara, CA. (800) 452-4844. **Circle No. 560**

The MathWorks Inc, Natick, MA. (508) 653-1415. **Circle No. 561**

Spectron takes over Microsoft RMI development

Spectron Microsystems has assumed development and support responsibility for the Resource Manager Interface (RMI) from Microsoft Corp (Redmond, WA). RMI, a joint development of Microsoft and Spectron, provides a signal-processing, hardware-independent driver for Windows applications using standard Microsoft application-programming interfaces (APIs). RMI enables these applications to access real-time services from a Pentium host processor or from various vendors' DSPs. Spectron will continue the drive to establish the RMI, a de facto standard, as an open standard by offering it to all industry participants. The company plans to deliver RMI-based drivers for Windows APIs, such as Wave and Telephony API. Meanwhile, Microsoft will focus on higher level APIs to support multimedia and telephony applications.—by Fran Granville

Spectron Microsystems, Goleta, CA, (805) 968-5100. **Circle No. 562**

Low-voltage device marks trend for analog ICs

At the International Solid State Circuits Conference three weeks ago, Analog Devices demonstrated an IC that exemplifies a trend for low-voltage analog ICs. By incorporating complex subsystems within a single IC, these devices are following the same integration path that digital ICs did as they migrated from 5 to 3V operation. For analog ICs, the difficult barriers to such higher levels of integration with the reduced supply voltage are lower signal headroom and S/N ratio, increased on-chip crosstalk, and the ability to maintain analog performance over various operating conditions. For designers, such increased functionality offers mixed-signal ASICs that suit one application. Such ASICs reduce the need for interconnecting and debugging separate small-scale IC designs and provides guaranteed system-level specifications. As an added benefit, these ASICs more efficiently handle broader system-level issues, such as power management and various subsection power-down modes. Finally, such

(continued on pg 16)

complex, low-voltage analog ICs suit true 3V-nominal operation, operating down to 2.7V.

The new IC, AD7015, suits digital cellular phones supporting Global System for Mobile, DCS1800, and PCS1900 standards. It has three major subsections, which had previously required separate ICs. A voiceband codec connects the microphone and ear piece to the phone's DSP and includes a 16-bit DAC, a 16-bit ADC, and programmable gain amplifiers. A baseband codec for the IF stages between the DSP and phone has a burst memory and Gaussian minimum-shift-keying modulator, two 10-bit DACs and their reconstruction filters, and two sampling 15-bit ADCs and associated digital filters. For the auxiliary functions, such as frequency control, power control, and signal-strength and battery monitoring, the IC also has four control DACs and a three-channel, 10-bit ADC. The device is sampling now; volume units will be available in midyear for $13 (OEM).

—by Bill Schweber

Analog Devices Inc, Wilmington, MA, (617) 937-1428. **Circle No. 563**

Quake to shake semiconductor industry?

In the early morning of Tuesday, Jan 17, an earthquake registering over 7.2 on the Richter scale roared through Kansai, a major economic province in central Japan. Kansai reportedly is responsible for more than 18% of Japan's domestic output and home to several semiconductor-, computer-, and electronics-manufacturing concerns. Although human suffering is extensive, the tremor's impact on Japan's semiconductor industry seems, initially, small, compared to the overall scope of the disaster.

The full extent of damage to semiconductor-manufacturing facilities is as yet undetermined, but preliminary reports include the following:

- Display Tech, a Toshiba-IBM joint venture that manufactures LCDs for PCs, shut down for about a week to repair the production line.
- Hoshi Electric, an LCD manufacturer in West Kobe, shut down its clean room when the earthquake hit.
- KTI Semiconductor, a joint venture between TI and Kobe Steel in Nishiwaki (west of Kobe), received no structural damage, but the quake dislodged production equipment from its mounts. Production is on hold, pending repositioning and recalibration of equipment.
- Matshushita-Kobe, a word-processor and PC plant, closed due to flooding from broken water pipes.
- Mitsubishi Electric operates five plants and labs in the Kansai area, accounting for 40% of the company's production. There is reportedly major damage, plus problems from lack of power and water, and an inability for employees to commute. However, the

(continued on pg 18)

TOUCH MONITOR COMBINES AUDIO SYSTEM, HIGH-CONTRAST DISPLAY

The Mac n' Touch AV-14 touch monitor from MicroTouch combines the vendor's ClearTek 2000 smart touchscreen, an ADP/SMT surface-mount touchscreen controller, and a 14-in. Apple AudioVision monitor, which includes stereo speakers and a microphone. The monitor provides a 0.28-mm dot pitch, a 1024×768-pixel video-display resolution, and a 1024×1024-pixel touchscreen resolution. The ADB/SMT controller comes in a 3.75×2.5×0.9-in. plastic box that mounts on the back of the monitor.

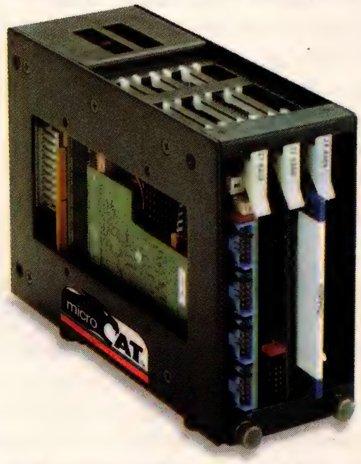
MicroTouch's Mac n' Touch touch monitor combines the vendor's ClearTek 2000 smart touchscreen, an ADP/SMT surface-mount touchscreen controller, and a 14-in. Apple AudioVision monitor, which includes stereo speakers and a microphone.

The monitor suits use in kiosks and computer-based training. Kiosk users are often untrained, and touchscreens are more user-friendly, tamper-proof, durable, and reliable than are other input devices, such as keyboards, mice, trackballs, and pushbuttons, according to the company. Touchscreens in training applications let users retain information because they spend more time interacting with a system rather than learning how to use it. Developers of multimedia applications can plug the touchscreen cable into the ADP port and load the touchscreen driver on a Macintosh, making any Mac application touch-activated. The AV-14 costs $1610.

—by Fran Granville

MicroTouch Systems Inc, Methuen, MA, (508) 659-9000. Circle No. 564

DON'T PUSSYFOOT AROUND!



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company's main memory business is not in the quake zone.

- NEC (Ohtsu), maker of 4-Mbyte DRAMs, resumed production the evening of the quake, although nearly half the staff could not attend work on the day of the quake.

The immediate effect of the quake on the semiconductor market was a slight spike in prices. Memory chips reportedly rose about 3% as quake-related speculation swept the "gray market," which is trading among US companies that buy and sell PC equipment. Less certain are the longer term effects due to interrupted supply lines. The quake severely damaged the transportation infrastructure, toppling freeways, suspending train operation, and closing airports and harbors.

Workforce disruption may also play a factor in semiconductor manufacture. So far, 5000 people have reportedly been killed. Tens of thousands were injured, and more than 200,000 people are homeless.

In addition to the quake's impact on Japanese semiconductor production, there many now be a need to take a second look at the earthquake's impact on Japan as a *market*. The Japanese Federal Budget plays a large role in determining the strength of the Japanese market for semiconductors. That budget, which must now accommodate up to $30 billion in disaster relief, will take effect in April. The Diet, Japan's parliament, has assembled to discuss the situation.—by Rich Lehtinen, Maria Tseng, Bert McComas, Ray Jodoin, Tony Massimini, and Morry Marshall, Contributing Analysts, In-Stat

In-Stat, Scottsdale, AZ, (602) 483-4440. **Circle No. 565**

HEURIKON GIVES COMPANY INFO—AND CARTOONS—ON THE INTERNET

Heurikon's HomePage for the Internet provides interactive on-line access to information about the company's facilities, products, and services. To entertain customers, Heurikon's HomePage will also feature a daily cartoon from Madison, WI, cartoonist PS Mueller.

The HomePage, hosted on a Unix-based World Wide Web Server, employs a point-and-click graphical user interface. By selecting the appropriate icon, customers can quickly access collateral materials, such as press releases, data sheets, and white papers. Soon, customers will be able to use the HomePage to take a factory tour and peruse the company's newsletter, *On the Bus*. World Wide Web also provides links to other company's HomePages, letting customers obtain information about Heurikon's third-party vendors. HomePages from Integrated Systems Inc, Intel, Mips, Motorola, and Silicon Graphics link to Heurikon's HomePage. Heurikon's HomePage address on the Internet is HTTP: www.Heurikon.com. —by Fran Granville

Heurikon Corp, Madison, WI, (608) 831-5500.
Circle No. 566

NEMA adopts IEC standards. The National Electrical Manufacturers Association (NEMA) has released three standards publications, IA 2.1, 2.2, and 2.3. The publications reflect NEMA's adoption of the International Electrotechnical Commission's five-part standard 1131 with deviations to accommodate the National Electric Code and its US practices. ANSI also recently adopted NEMA standards. The three standards publications are "NEMA IA 2.1/IEC 1131-1—General Information," Catalog No. 10006 ($70); "NEMA IA 2.2/IEC 1131-2—Equipment Requirements," Catalog No. 70007 ($195); and "NEMA IA 2.3/IEC 1131-3—Languages," Catalog No. 10008 ($280).

National Electrical Manufacturers Association, Washington, DC, (202) 457-8400.
Circle No. 567

VHDL-synthesis tool suits first-time FPGA users

The ACTmap VHDL-synthesis tool from Actel provides a high-level design environment for first-time users of field-programmable gate arrays (FPGAs) and VHDL. Actel developed the tool using core technology the company licensed from Innovative Synthesis Technology. Based on architecture-specific algorithms, the IEEE 1076-compliant synthesis tool offers designers a boost in productivity and shorter time to market, according to the company.

The tool features interfaces to popular CAE tools for block-level design or reoptimization, automatic inference of arithmetic operators, tristate mapping to Actel multiplexers, and one-hot and compact encoding to maximize state-machine performance. The Designer Series starts at $995 for new customers. Actel incorporates the Windows-based system into its Designer Series FPGA-development systems at no extra cost. Users that have Action Logic Systems can upgrade to the Designer Series FPGA by purchasing a $495 upgrade that includes ACTmap VHDL synthesis, ACTgen macro builder, the ChipEdit placement editor, and Actel's Windows-based user interface.—by Fran Granville

Actel Corp, Sunnyvale, CA, (408) 739-1010.
Circle No. 568

Videos cover RAID technology. Three videos from the RAID Advisory Board (RAB) highlight redundant-array-of-inexpensive-disks (RAID) technology. "Raid Basics" ($195) provides a 10-minute overview of the technology and the seven Berkeley RAID levels. The 7-minute "RAID Futures" ($285) details what RAID technology will look like by 2000. The 5-minute "RAID Advisory Board" ($10) covers the goals, members, and achievements of RAB, which has more than 50 member companies.

RAB Advisory Board, St Peter, MN, (507) 931-0967. **Circle No. 569**

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CIRCLE NO. 49

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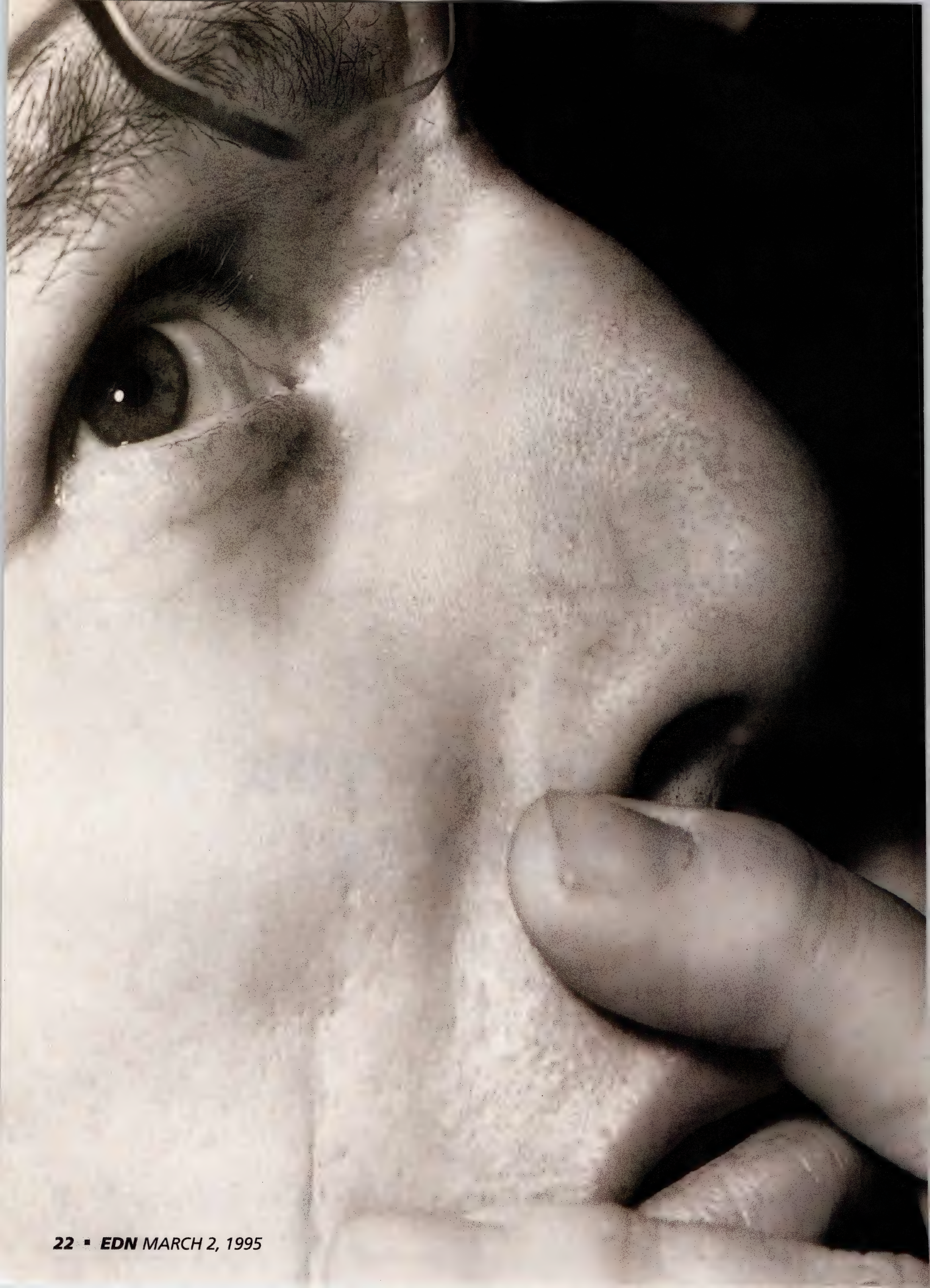

EDITORIAL | OPINION

Revisiting Decade 90: fault-tolerant design

In early 1988, I wrote a five-part series called "Decade 90: the future of system design." In it, I tried to forecast the major technological trends that would shape our industry in the 1990s. This is the last in a series of five mid-decade editorials looking at how close the predictions came.

Military and aerospace systems have used and continue to use fault-tolerant designs, but commercial, industrial, and consumer products have not followed, for three reasons. First, the reliability of conventional electronic hardware is constantly improving, so the added cost and complexity of fault-tolerant design is unwarranted. Processors have MTBF ratings in the hundreds of years, and memories no longer suffer as much from soft errors. Further, increasing levels of integration have ushered in the era of single-chip systems, and surface-mount assembly with its automated production has caused a tremendous improvement in large-system reliability. Sensor-based feedback systems compensate for wear and tear without resorting to redundant fault-tolerant design.

Second, the increasing pace of innovation in the electronics industry has dramatically shortened the useful life of most electronic products. Five-year life cycles have become the exception. In fact, newer, more efficient electronic equipment comes along to replace older units before the older units reach the end of the constantly receding reliability curve. Companies must either ride the technological wave by constantly upgrading equipment or wipe out and let the competition overtake them.

Third, the competitive '90s attitude precludes companies from employing design strategies that add cost but not "value." Few customers are willing to pay substantially more money for unstoppable hardware, but many will pay extra for more performance. For example, fault-tolerant design has taken hold in the market for redundant arrays of inexpensive disks (RAID) (*EDN*, Nov 24, 1994, pg 81). RAID systems gang multiple hard-disk drives, thus realizing the combined benefits of higher throughput and fault tolerance. Because disk drives are electromechanical, they are less reliable than are purely electronic systems. As such, disk subsystems can benefit from fault-tolerant design techniques. Even hard-disk reliability has skyrocketed in the last couple of years, however. Fault tolerance has succeeded in RAID designs but failed to catch on elsewhere because RAID is one application in which fault tolerance also delivers improved performance, thus providing sufficient value to justify the expense. (I was not farsighted enough to mention RAID in my "Decade 90" article on fault tolerance.)

If you've been keeping score over these last five editorials, you may have noticed that the "Decade 90" series did a good job of predicting development, at least from the mid-decade perspective. Although we've seen a lot of innovation, many things haven't changed. ICs still use transistors—albeit much smaller transistors these days—and digital circuits still employ binary coding and signaling schemes. We still solder ICs to circuit boards, though through-hole technology is rapidly going the way of tube sockets and discrete, handcrafted wiring.

I'm not prepared to write a "Millennium 3" series of prognostications just yet, but I will point out a few interesting and revolutionary developments on the horizon. Quantum-line and -dot semiconductors and polymer (plastic) transistors are already working in laboratories. K Eric Drexler's visions of nanomachines increasingly haunt my dreams, spelling the possible end of the electronics age (at least as we know it) early in the next century. The one black hole in all of this future tech is software. I don't care what the object-oriented advocates say; we're still in the software Stone Age. No matter what technology we use to build hardware, software will be around for a while.

If you have any insights into the Third Millennium, I'd be interested in hearing from you.

EDITOR IN CHIEF

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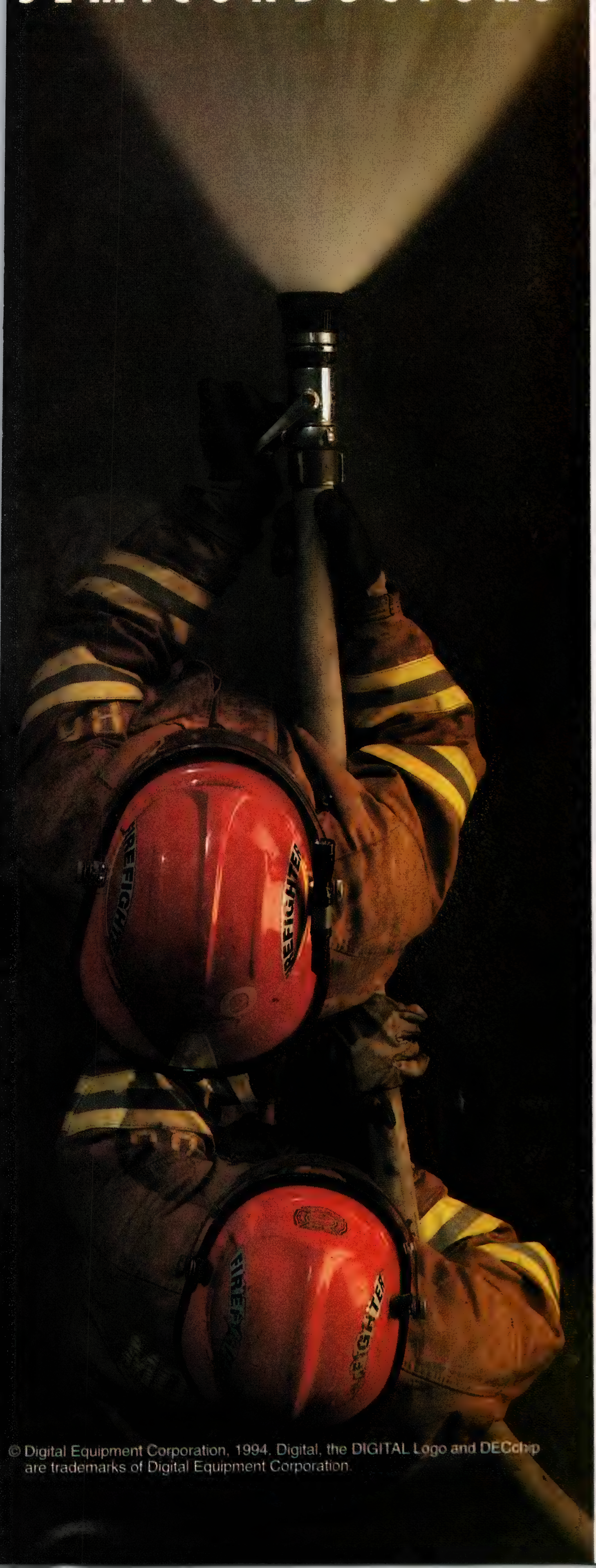

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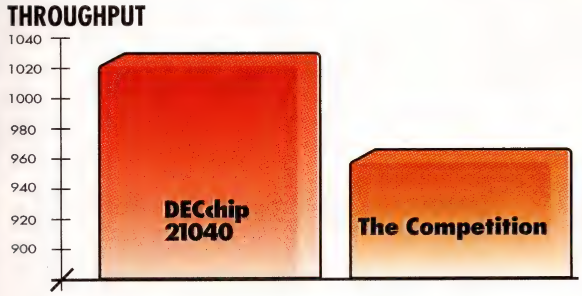

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CIRCLE NO. 37

Innovation correction

We're excited over Chip Express's selection for your 1994 Innovation Awards in the IC and Semiconductor product of the year category. Upon reading the description of our OneMask technology on page 42 of your February 2 issue, we have noted an inconsistency from the materials we submitted.

The OneMask capability is currently available not only in 1.2-μm double-layer CMOS in gate counts from 2000 to 18,000 gates but also in 0.8-mm double-layer CMOS with densities from 10,000 to 80,000 gates.

Bob Sandler
Director of Marketing
Chip Express
Santa Clara, CA

Waste not, want not

Like most engineers, my time is precious. When I find the time to read, I must decide which of the excellent technical articles in *EDN* are most relevant to my career—and I read only them. The problem with Steven Leibson's editorial, "Irrelevant choices" (*EDN*, November 23, 1994, pg 45) is that it was an irrelevant choice. Thanks for your advice; I will strive to avoid irrelevance in the future.

Michael Friends
Interpoint
Redmond, WA

BiCMOS article misses the mark

The case for BiCMOS as a PLD technology choice is definitely unproven. Ron Cline's recent article, "Get ready to design with new-generation, BiCMOS-based 3.3V PLDs" (*EDN*, October 27, 1994, pg 117), promotes BiCMOS with internal ECL and fuse technology as the answer for fast, 3.3V PLDs.

This could hardly be considered a step up in value for small-sized PLD customers. BiCMOS has long been a technology looking for an application to justify its added complexity and cost. Small PLDs are not that application.

Does the article describe parts with low power levels expected with 3V operation? Power is not mentioned, but ECL circuit technology is not noted for achieving low-power designs.

The design described in the article also uses fuse technology for the programmable elements. A fuse technology was most likely chosen to minimize the MOS requirements of the BiCMOS process. Reprogrammability and, more important, unlimited testability were sacrificed by the fuse technology choice.

So, what does BiCMOS bring to the 3.3V party? For now, and what appears to be the immediate future, nothing that CMOS cannot provide. EECMOS offers reprogrammability, testability, low ground bounce, leading-edge performance, and low power at 3.3V.

In June of last year, Advanced Micro Devices introduced an EECMOS (0.65 μm), 100-MHz, 7.5-nsec, 75-mA, 5V signal-compatible PALLV22V10-7. A next-generation EECMOS process ensures a path for further performance improvements for 3.3V PLDs at AMD.

William H Sievers
Advanced Micro Devices
Sunnyvale, CA

Sound off

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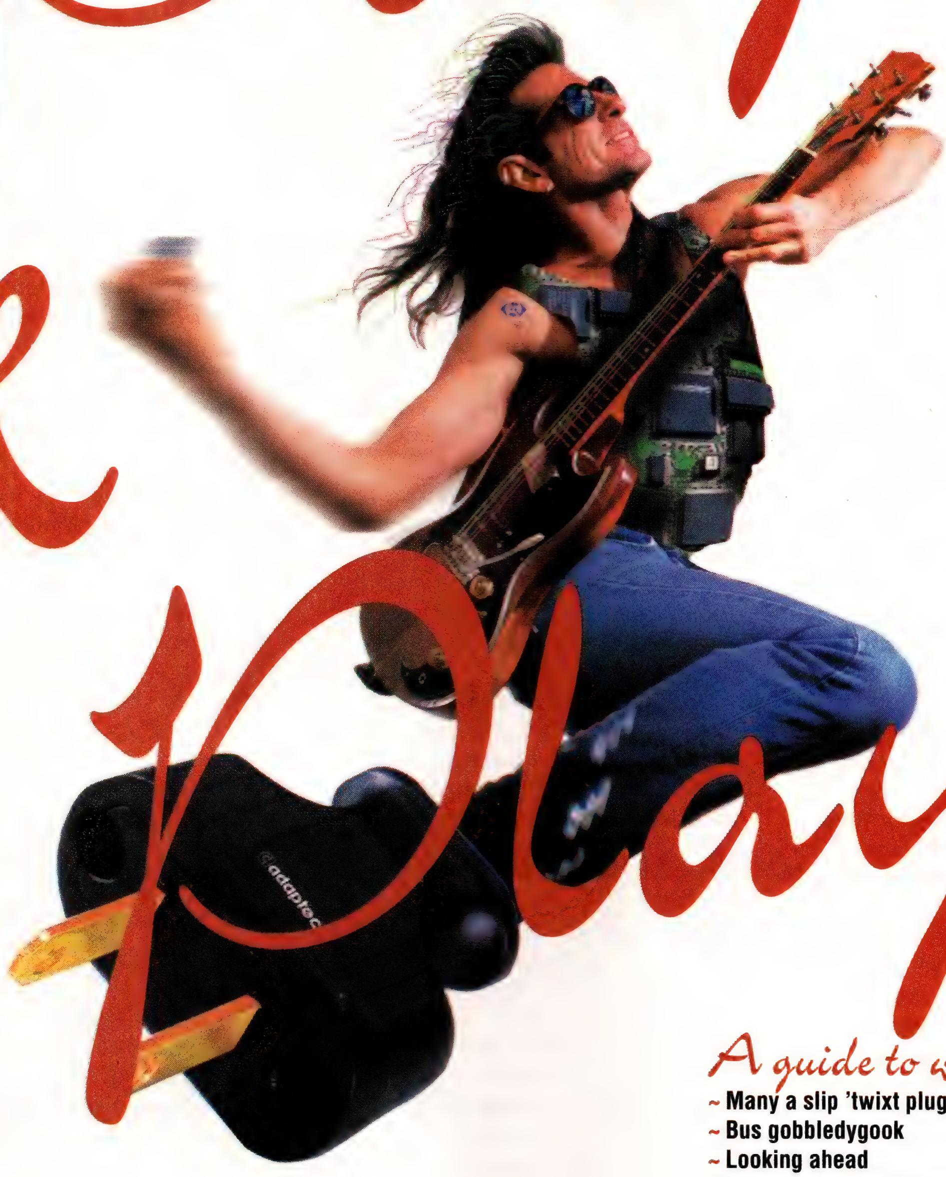
Plug & Play



Some say, a year after Windows 95 ships, PC users won't recall the agony of configuring I/O-board jumpers or DIP switches. Maybe. But before "plug and pray" yields to plug-and-play, vendors must begin to cooperate, and users must forsake 150 million legacy boards as well as the software that runs them.

A guide to what's inside:

DAN STRASSBERG, SENIOR TECHNICAL EDITOR

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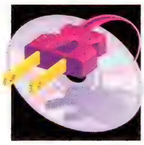
MANY A SLIP 'TWIXT PLUGGING AND PLAYING



In nearly every segment of the PC industry, people are hard at work on a group of initiatives known as Plug-and-Play (PnP), an umbrella term for a design philosophy that aims to make PCs easier to set up and thus accessible to a wider audience. While the best known PnP initiatives cover PCI, PCMCIA, and the venerable ISA bus, others cover such buses as EISA, SCSI, and VL. For a quick acronym review, see **box**, "Bus gobbledygook," a glossary that decodes these bus names. There are even PnP initiatives (Access.bus, for example) that deal with parallel and serial ports, external modems, monitors, and mice. Nevertheless, although PnP proponents have good reason for optimism, few of them should declare victory just yet.

Although hardly anyone thinks that much is right about the current trial-and-error method of assigning resources when installing PC peripherals, the industry's challenge is to implement a *practical* system of automatic resource allocation. (For ISA bus cards, the resources are interrupt-request lines (IRQs), DMA channels, memory-address space occupied by the card firmware, and I/O-port addresses.) The trial-and-error approach involves repeatedly restarting the system after trying to find the right jumper- and DIP-switch settings on I/O cards. Often, it also involves trying several software drivers and configuration options in applications packages. This approach, dubbed "plug and pray" by industry wags and "plug and hope" by Intel's more politically correct marketers, is a holdover from PC's early-1980s origins.

Under Windows 95, the operating system (OS) allocates the resources. Windows NT (including versions for µPs from vendors other than Intel) and IBM's OS/2 (IBM calls its latest release OS/2 Warp) also handle resource allocation. Other OSs for computers that use buses covered by PnP initiatives will follow suit. Add-ons will impart a subset of Windows 95's PnP capabilities to Windows 3.1, but Microsoft would prefer to see Windows 3.1 users upgrade to Windows 95 rather than add onto the older version. The software giant is thus almost certain to use Windows 95's more extensive PnP capabilities to convince users to upgrade.

Having the OS take care of resource allocation is technically elegant, but in the PC business, elegance doesn't necessarily equate with success. What nearly always prevails is marketing clout. Luckily, the prime movers behind several of the PnP initiatives (the ones for ISA, PCI, and PCMCIA) are

Microsoft and Intel. These two industry giants pack all of the clout imaginable. Scores of other companies that believe in PnP are cooperating. Representatives of smaller companies think that being first, or among the first, to market PnP products will give them a competitive edge, whereas failing to deliver such products when Microsoft first ships Windows 95 or shortly thereafter could be fatal.

Memories of failed attempts

But hanging over these initiatives are memories of failed attempts to rectify PC shortcomings. The MicroChannel bus of IBM's PS/2 line is an example. Though technically superior to ISA, it never achieved critical mass. When the introduction of a new technology is imminent, vendors and trade journalists often set PC users' expectations unrealistically high. A technology that falls short of user expectations when it first appears rarely gets a second chance, regardless of its merits. In the case of PnP, a prolonged "teething period" is likely. One reason for this is that many pieces must fit into place to make PnP work. A second reason is that there is an enormous legacy of software and hardware that predates PnP standards. ISA hardware is by no means the only offender.

Playing roles in making a system plug-and-play-configurable are the system BIOS firmware that resides in ROM chips on the system motherboard (BIOS stands for basic input/output system), the OS, the device drivers, the host-system hardware, the I/O card hardware and firmware, and even the application software. ISA PnP's architects carefully considered these factors in order to design a system that is backward-compatible with old hardware and, in some cases, with old software. (See box, "PnP—what does it take?")

Nevertheless, unlike systems whose elements all support PnP, most systems that contain a mixture of PnP and legacy elements offer relatively few advantages over systems that completely lack PnP support. (Certain elements are more important to PnP operation than

BUS GOBBLEDYGOOK

EISA—extended industry-standard architecture
ISA—industry-standard architecture
PCI—peripheral-component interconnect
PCMCIA—Personal Computer Memory Card International Association
SCSI—small-computer standard interface
VL—Video Electronics Standards Association (local bus)

Notes: 1. Notwithstanding the use of several of the listed buses in systems based on µPs not from the X86 family (as well as in X86-based systems), this article refers to the listed buses collectively as "PC buses."
2. Even though IBM PS/2 systems that use the MicroChannel bus are PCs—they use X86 µPs and run MS-DOS—the term "PC buses," as used here, does not include MicroChannel, for PC buses have open architectures. IBM controls the MicroChannel standard.

ILLUSTRATION / DANIEL GUIDERA

others; for example, a system can derive significant PnP benefits without using a PnP monitor or mouse.) The danger is that resellers may unwittingly supply systems that include one or more legacy elements and that users will become frustrated or angry when they find that an installation procedure they perceived as straightforward turns ugly.

PCMCIA is a case in point. The standard for credit-card-sized storage devices and I/O adapters was billed as a plug-and-play standard almost from the outset, but purchasers of notebook PCs soon learned otherwise. Eighteen months ago, nearly all purchasers of such PCs found that, to obtain PCMCIA cards that would work in their machines, they had to select from a very short list, which was published by the PC's manufacturer. These problems haven't derailed PCMCIA; its potential value is just too great. Moreover, by now, vendors have worked out most of the kinks. Often, though, older PCs require upgrades if they are to work with more than a handful of PCMCIA peripherals.

The situation with credit-card-size peripherals will become more complex with the introduction of a new bus that, although it still has no official name, seems destined to be called Cardbus. Although current PCMCIA cards will work in Cardbus "drives" (the slots into which you plug the cards), existing PCMCIA drives won't accept Cardbus cards. These new cards, with sizes the same as those of existing PCMCIA cards, will also have 68-pin connectors, albeit ones that have been modified to meet the needs of the faster bus. Just as PCMCIA is, in effect, a miniaturized ISA bus, Cardbus will be a sort of miniature PCI. Cardbus will be faster than PCMCIA, but not as fast as PCI, because Cardbus's narrower width requires transmission of data and addresses in 16-bit chunks. A Cardbus drive will sense whether a PCMCIA card or a Cardbus card has been inserted, and it will configure itself accordingly. This dual personality adds a new wrinkle to the PnP concept.

For some, PnP was easy

Not all systems have encountered the kind of difficulties in providing plug-and-play configurability that PCMCIA has experienced. Several buses have offered plug-and-play operation from the outset—and have done so with little fuss or fanfare. Two such buses are the Macintosh's Nubus and the MicroChannel bus. These are the most widely distributed embodiments of plug-and-play technology. But many lesser-known systems—mostly ones that use proprietary buses, where a single company controls the hardware and software—have offered plug-and-play features for more than a decade.

The ISA bus differs in one important aspect from the MicroChannel bus, the Macintosh implementation of the Nubus, and the proprietary systems. In all of these systems except ISA, even where there are multiple vendors, one company controls the hardware and at least some key part of the software. For example, IBM PS/2 systems so far seem to come close to achieving full plug-and-play capability only when running the company's OS/2 OS. PC buses, on the other hand, are truly open, multivendor architectures.

Making PnP work in the multivendor PC environment requires cooperation from all of the vendors. Such cooperation is difficult to achieve because many of the companies involved are direct competitors. Microsoft, despite its dominance in the PC-software industry,

Looking Ahead

The success of Plug-and-Play is *not* a sure thing. Still, with Microsoft and Intel behind PnP, a company in the PC hardware or software business would be foolish not to support it. Consider the downside of supporting failed PnP initiatives vs the downside of not supporting successful ones. If PnP fails, a company that has supported it will have wasted some product-development money and will have products that cost slightly more than they would cost without PnP support. On the other hand, if PnP succeeds, a company that misses the PnP window loses almost all of its market share and probably can't stay in business long enough to bring PnP products to market. If those really are the alternatives, supporting PnP is the only rational course.

If vendors view the issues in this light, a flood of PnP products will hit the market in 1995—assuming that Microsoft ships Windows 95 early enough for resellers to deliver significant quantities to users this year. (To date, Microsoft has slipped the shipping date to August, although skeptics continue to speculate on the possibility of further delays.) If the manufacturers properly verify their products' PnP capabilities so that even the first units shipped perform to customers' expectations, PnP will be a runaway success and PnP support will become absolutely necessary in all new hardware and software products for PCs.

In fact, if PnP becomes a standard feature of PCs but not of workstations, workstation vendors will come under substantial pressure to implement PnP before they lose even more market share to PCs. Although, on average, workstation users are much more technically sophisticated than PC users (and thus need PnP much less), they aren't immune to sales pitches based on ease of use. According to one survey, over half of the potential workstation buyers consider acquiring PCs instead of workstations. Coincidentally, these are the buyers who can benefit most from PnP. Thus, the low end of the workstation market is particularly vulnerable to competition from PnP PCs.

But if PnP goes down in flames, the big beneficiary will likely be the Mac. So far, the abundance of software for X86-based PCs has enabled these machines to capture over 90% of the PC market, even though they lack plug-and-play features the Mac offers. This situation is the result of X86 machines' open architecture. But the Microsoft/Intel push for PnP will increase public awareness of the need for plug-and-play. Buyers who perceive that an all-out push to create a PnP environment on X86 PCs has failed are likely to embrace the original plug-and-play PC—the Mac, or its successor, the PowerMac. In that event, the timing of Apple's belated and reluctant attempt to open the Mac architecture may look like a stroke of genius.

does not exercise complete control over the PC business. In hardware, the number of computer and peripheral suppliers is in the hundreds—if not the thousands. Microsoft supplies very little hardware; its best-known hardware item is the Microsoft Mouse.

In software, notwithstanding Microsoft's leadership in sales of PC OSs, PC users can opt for OSs from other vendors, including IBM. (OS/2 is not restricted to PS/2 systems; it runs on most PCs that use 32-bit X86 μPs.) In PC application software, where Microsoft is also the largest player, competition is even more intense. In PC BIOS firmware, there are at least four major vendors and many smaller ones; Microsoft does not supply BIOS code.

After a long period of seeming not to care about plug-and-play, Microsoft wants PC users to have it and have it *now*. The reasons are clear. After many false starts, home-PC applications are finally emerging as a key area of potential growth for PCs. Among home applications, multimedia is very important, and no type of PC hardware has caused more installation headaches than multimedia hardware.

Plug-in expansion is here to stay

Despite the high risk of encountering major hassles when users or support people try to add hardware options to PCs, plug-in hardware expansion will remain a fact of life in the PC world. Installation problems (as well as fears of experiencing them) are inhibiting the next phase of PC-market growth, however. Home users can't deal with configuration hassles, and with the thin margins on PC products, vendors, including giants such as Microsoft, can't afford to hold users' hands.

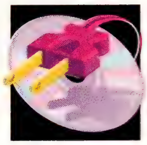
Meanwhile, easily swapped hardware modules, such as PCMCIA cards and external SCSI devices, add yet another dimension to the configuration problem—the need to support dynamic reconfiguration. Similar problems arise from notebook PCs' ability—while under power—to plug into and unplug from desktop units that contain more and different system elements (higher resolution displays, for example). Hardly anyone wants to think about what happens when a user disconnects a hard disk containing the memory overlays for a currently running application. Although the situation is analogous to removing the program diskette from an old floppy-disk-based PC (something that rarely caused a crash), one developer likes PCs that can tolerate removal of their program-storage media to fault-tolerant computers of the type found in the banking industry's on-line transaction processors. Such systems aren't PC-based.

At least for now, users should be careful about unplugging removable devices that are in use. When a PC's modem is not on line—even if the communications software is running—it's probably safe to pull a PCMCIA modem out of a notebook PC. But removing a storage device that contains executable portions of the OS or of a running application invites a system crash.

Eventually, such precautions should become unnecessary. Not only OSs, but also application software will be PnP-aware. A RAM-resident portion of the OS will detect that you've removed a hardware element and will pass a message to the application. Upon receiving the message, the application will know not to access the missing element. If the removed item is a memory device containing part of the application code, enough of the application will remain in RAM to keep it from crashing, should you attempt to access the missing system element. Moreover, the OS will display a message asking you to replace the missing item. If you indicate that you do not wish to do so, the OS will suspend or shut down the application.

This is just one example of the cooperation among diverse system elements—both hardware and software—that must exist for PnP to succeed. The complexity of today's hardware and software places major obstacles in the way of PnP. As with so many aspects of today's computing systems, the possibilities that developers will overlook small, but critical, elements are virtually unlimited. In addition, the chances of figuring out in advance all of the combinations of events that must be tested to guarantee reliability seem minuscule.

PNP—WHAT DOES IT TAKE?



To make PnP practical in an environment that allows unlimited numbers of board types from an almost-unlimited number of vendors, strict standards must exist on the boards' behavior. When you first install it, a PnP board isolates itself from the system. In other words, the board listens for messages intended for it, but it does not place data on the bus until asked. Until configuration is complete, that data could conflict with data sent by another system element.

In any PC, the BIOS code executes immediately after you apply power. A PnP BIOS is an important part of a PnP system. The roles of the BIOS and the OS are closely linked; in fact, they overlap. Just which functions are performed by BIOS code and which are performed by the OS depends on both the BIOS and the OS. For example, Windows 95 will run with certain limitations in PCs that lack a PnP BIOS. When Windows 95 runs in a PC that includes a PnP BIOS, the OS performs several functions that BIOS code might perform under another OS. Nevertheless, Microsoft feels so strongly about the need for a PnP BIOS in Windows 95 systems that it plans to require such a BIOS in every PC that carries the Windows 95 logo.

Under Windows 95, the BIOS's role in PnP is to identify and configure the boot devices—ones that must be present for the OS to load into RAM. Besides the hard drive or other mass-storage device, the boot devices are the display, an input device (usually the

keyboard), and, on diskless workstations, a network adapter. A non-PnP BIOS makes replacing such system elements much more difficult. The following discussion applies to systems running under Windows 95.

After finding a minimal hardware configuration, the BIOS passes control to the OS, specifically to an OS module named the configuration manager (CM). The CM calls additional software modules known as enumerators to locate and identify the devices on each bus in the PC. PnP boards report what system resources they can use and inform the enumerator of their manufacturer and type. The OS needs to know a board's exact identity so it can install the correct software driver or—if it can't locate the driver in mass storage—can ask you to load the driver. The CM also checks for additional information in a registry file on the PC's hard disk or flash EEPROM. This file contains the particular PC's configuration history.

Building a tree

The CM then constructs a hardware tree reflecting the PC's current configuration and calls software modules known as resource arbitrators to resolve conflicts and dynamically reassign resources. The arbitrators need to be aware of dependencies (for example, a modem card assigned to COM1 uses IRQ4; the same card, assigned to COM2, uses IRQ3). Finally, the OS configures and installs the appropriate device drivers.

Where possible, the OS assigns the resources in a way that does not create conflicts. You can, however, install hardware combinations that create irreconcilable conflicts. When this happens, PnP eases the pain. The OS informs you of which devices conflict, and you can tell the OS which devices to ignore in the current session. Maybe you won't be using your document scanner for a few hours. If so, you can disable it and enable your sound card. Later, when you need the scanner but not the sound card, you can invoke the CM and alter your selections without rebooting.

From the preceding discussion, you

FOR FREE INFORMATION

The companies and organizations listed below provided material used in preparing this article; they are representative of the hundreds of companies that support various PnP initiatives. For information on their Plug-and-Play products, publications, or activities, circle the appropriate numbers on the postage-paid Information Retrieval Service card or use *EDN*'s Express Request service. When you contact any of the following companies or organizations directly, let them know you read about them in *EDN*.

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probably understand that, despite the central role of software in PnP, a PnP board must incorporate some fairly complex logic. The cost of incorporating this logic is not extreme, however. The usual route is to add the logic to an ASIC you develop for the board. Several ASIC vendors offer the necessary logic in their cell libraries. At least two companies, Fujitsu and National Semiconductor, offer dedicated ISA bus PnP controller chips. Fujitsu's MB86701, in a 120-pin PQFP (plastic quad flatpack), costs $5.95 (10,000). The EVA 86701 evaluation kit, an Ethernet card with network drivers and utilities, costs $159.

With buses to which you can make external connections (two examples are PCMCIA and SCSI), hot swapping is an issue. Also, many notebook PCs support hot docking (power-on insertion of the PC into a docking station that can contain additional system elements). Where these possibilities exist, the bus controllers must poll the bus slots periodically to determine whether boards that were in the system are still present and whether new boards have been added. If a bus controller detects a change in the installed hardware, it must pass a message to the OS. In systems that permit neither hot swapping nor hot docking, polling of the slots needs to take place only when the system first powers up.

Hot swapping and hot docking require use of special connectors that first make a ground connection and then make power-supply connections. Signals are connected only after the power supplies are stable. Moreover, just before you plug a unit into a powered-up bus or docking station, the bypass capacitors in the unpowered unit are usually discharged. Unless the unit's design limits it, the flow of charging current through the impedance of power-supply and ground lines can cause voltage spikes that interfere with the operation of other system elements.

Gotchas aplenty

Implicit in the description of how a PnP system configures itself are all sorts of "gotchas." For example, suppose a plug-in board's hardware conforms to the letter of the PnP standards but the vendor hasn't yet updated the software driver. The board can use any one of three IRQs; whereas the driver, which was written for an earlier board, assumes that one particular line will be assigned. Will the OS be smart enough to assign the one IRQ that works with the driver, or will it pick a line that is compatible with the board but not with the driver?

The architects of ISA PnP foresaw situations of this type and allow you to edit the hardware tree to force a compatible selection. The problem is that

editing the tree is a job for a knowledgeable user. Even the name—Plug-and-Play—implies that this kind of playing around won't be necessary.

Legacy hardware developed before the advent of PnP standards presents a huge challenge, and the standards address it. For the ISA bus, Intel has developed a database that, at last report, listed the resource requirements of 280 of the most popular legacy boards. If your system includes one of these boards, all you must do is inform the CM of the board's presence. The OS determines what resources you should assign. You may have to reset jumpers or switches, but, to make the board work, you shouldn't have to do so more than once.

PnP also handles another obvious problem—your system can easily include a legacy card that isn't in the database. Because some 10,000 types of ISA bus cards exist and the database covers fewer than 3% of them, handling cards not in the database is quite important. If you have the card's documentation, you can describe its resource requirements to the CM, and Windows 95 will allocate appropriate resources. In some cases, software may even determine the resource requirements of unknown boards. The ability to handle cards that aren't in the database is important for another reason: Many such cards are similar enough to ones in the database to be confused with them, yet different enough to require different resources.

Even boards for relatively new buses, such as PCI, can be troublesome. A widely held misconception is that all PCI boards support PnP. In fact, only boards that conform to Revision 2.0 or higher of the PCI spec support PnP. Some well-known vendors are still shipping PCI boards designed before PCI Rev 2.0 existed. PnP protocols don't configure these boards automatically. Nevertheless, PCI presents far fewer problems than ISA does and not only because there are relatively few legacy PCI boards. A PCI bus accommodates fewer boards than an ISA bus does. Moreover, because of PCI's greater speed and burst-mode transfer capabilities, a smaller percentage of PCI boards use interrupts and DMA. Thus, PCI reduces competition for these scarce resources.

PnP SCSI—TERMINATING THE MISERY

The SCSI bus is a high-speed bus that can connect to peripheral devices both within a computer's systems unit and external to it. For proper operation, the bus lines must be terminated at both ends; otherwise, reflections interfere with the bus signals. An unusual feature of the SCSI bus is that you can place the unit that originates the bus—the SCSI host adapter—anywhere on the bus; you needn't place it at one end.

Making sure that the terminations are at the two ends of the bus and only there has proven to be a nightmare for many computer users. Apple's Macintosh systems were the first PCs to use SCSI. According to one Apple supplier, 50% of the customer-support calls to Apple resellers relate to SCSI. Of those, 75% relate to improper termination.

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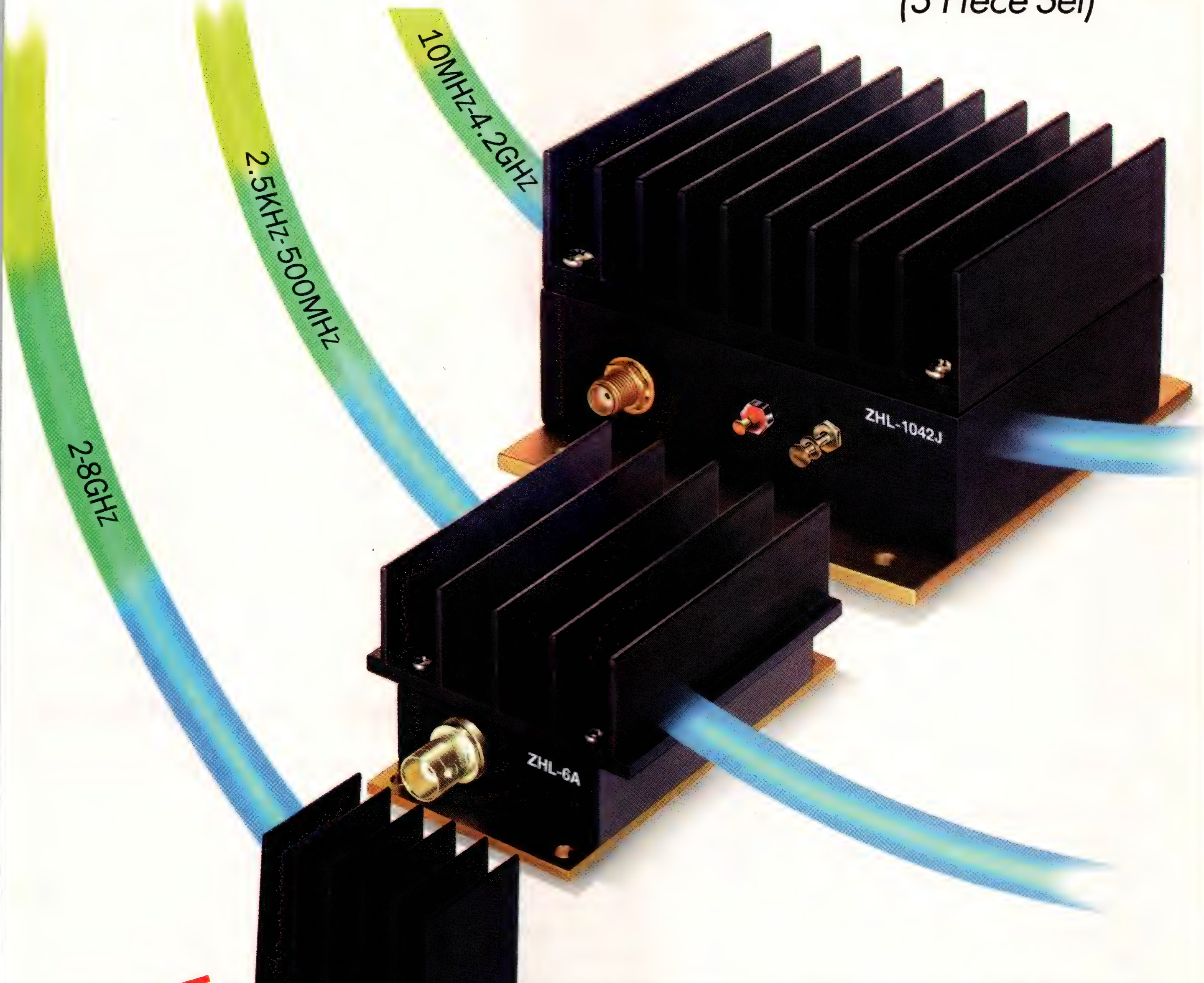

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In a generic sense, a SCSI bus has three possible physical arrangements:

- It can connect only to devices within the systems unit (hard-disk controllers, for example).
- It can connect only to devices outside the systems unit.
- It can connect to devices both within and outside the systems unit.

In the first two cases, one end of the bus is on the host adapter, so the host adapter must terminate its end of the bus. In the third case, neither end of the bus is on the host adapter, and the host adapter must not terminate the bus.

A single ribbon cable links the host adapter to all internal peripheral devices. A SCSI ribbon cable includes one connector for each internal device you might connect. In older SCSI systems, you had to plug a bus-termination network onto the last internal device in the chain. Older device boards include a place to plug in the network. Users who tried to reconfigure their systems (say, to add a peripheral) would often either forget to remove the termination from a device that was no longer at the end of the chain or were unable to locate a network to add to a device they were moving from the middle of the chain to the end.

Switchable terminators

Switchable termination networks improve on this situation somewhat. They are a permanent part of the peripheral device, so you can't lose them. But, until PnP, you still had to switch them into or out of the circuit. In PnP SCSI systems, the ribbon cables solve the termination problem for all internal SCSI devices except the host adapter. PnP ribbon cables include a termination network permanently attached to the cable's distal end (the end farther from the host adapter). With such a cable, you remove or switch off all of the internal SCSI devices' termination networks, except possibly the host adapter's. If the bus does not leave the systems unit, the host adapter must terminate its end of the bus.

The situation for external SCSI peripherals is a little different. Outside the systems unit, the SCSI bus uses round cables. Each external device includes a pair of connectors. One brings the bus to the device; the other accepts either a cable that carries the bus to the next device or (in older devices) a plug-

in bus-termination network. If an external device that includes a switchable terminating network is the last in the chain, the network is switched on, and the second connector is unoccupied.

PnP SCSI systems make concern over correct termination obsolete. Each external device determines whether it has one or two cables connected to it. The same is true of the host adapter. (The host adapter accommodates one external cable and one internal cable.) If two cables are connected, the terminator switches off automatically; if one cable is connected, the terminator switches on.

Termination networks are not SCSI PnP's only concern, however. The peripheral devices must be designed so that the host adapter can assign their bus addresses. In SCSI systems that contain older devices, you must assign the addresses yourself, using switches. If you assign the same address to two or more devices, the system will crash. PnP SCSI host adapters solve this problem using a facility in their firmware unhappily named SCAM (SCSI Configured AutoMatically). SCAM works even on SCSI buses to which you attach non-PnP devices. If you assign nonconflicting addresses to those devices and then add PnP devices, SCAM automatically assigns nonconflicting addresses to the PnP devices.

PLUG-AND-PLAY AND THE VMEBUS

JOHN RYNEARSON, VME INDUSTRY TRADE ASSOCIATION (VITA)

-Plug-and-play has come a long way since the early days of the VMEbus. Most early VMEbus boards required careful manual configuration before they were ready for installation in a system. Usually, switches or jumpers had to be set and various options selected manually. The installer's choices among options were not always clear and often caused inadvertent selection of conflicting options. In addition, the jumpers proved to be unreliable and susceptible to shock and vibration.

Several key features make play-and-play feasible. First, circuit boards must be designed with programmable registers instead of jumper blocks or manual switches. Then, as the system starts up, software can configure them. This approach transforms system configuration from a hardware problem to a software problem that is solvable by programming. Software programmability offers many advantages. Once a programmer determines the proper sequences, the software performs them the same way every time. Boards that are swapped in the field will automatically be configured correctly. Eliminating jumper blocks improves system reliability. Board test during manufacture can be more thorough and accurate: Software—rather than time-consuming, error-prone manual operations—can exercise all options.

Because of these advantages, board designers have moved away from jumper blocks and manual switches to programmable registers. In so doing, they have made plug-and-play possible. Many VMEbus interface chips provide a set of registers that are usable for setting various board options.

However, plug-and-play at this level requires unique software for each module, and it requires that the system integrator know, in advance, what boards will go into a system. The ultimate goal of plug-and-play is to dynamically determine if a particular board is present and, if it is, to provide

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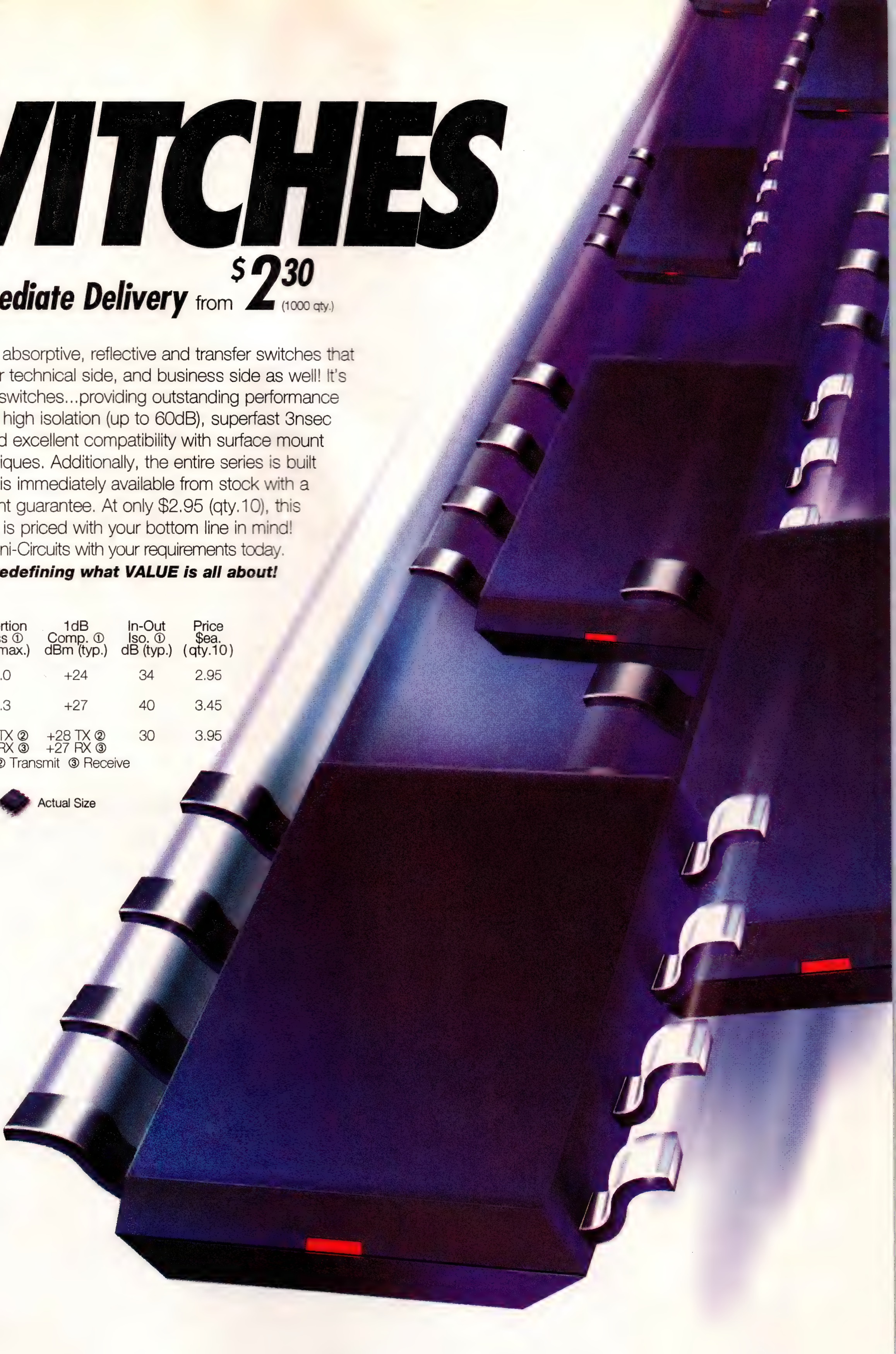

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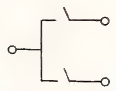

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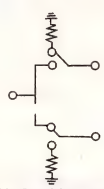

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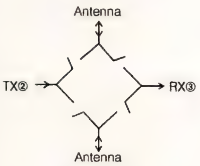

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the proper configuration.

The most common method a system uses to configure itself is to provide a unique address space that contains configuration ROM (CR) and command and status registers (CSR) for each module. During system boot, the software probes each module's CR/CSR space. If a module responds, the host CPU reads information from the ROM that indicates what board is present and how to configure it.

CR/CSR space holds the key to true plug-and-play operation. To make plug-and-play possible, the developers of the new VME64 specification include the concept of CR/CSR space. This unique address space provides a mechanism for manufacturer and board identification and automatic board initialization, configuration, and test. CR/CSR space is a also a key element in hot swapping of boards.

Many applications, such as telecommunications, require replacing suspect modules while the system remains under power. The new module must be initialized, and CR/CSR space allows the software to configure the board properly.

A goal of the VMEbus's open-bus technology has always been to make system integration as simple and as straightforward as possible. By adding CR/CSR space, the new VME64 specification serves this goal. The VITA 1-1994, VME64 specification is in the final stages of balloting and will be in the hands of ANSI for official recognition by the time you read this.

Two places to turn for help

The purpose of this article is to make you aware of the issues involved in PnP. If your job is to create a Plug-and-Play hardware or software product, the material here is just the beginning of what you need. The companies listed in the **box**, "For free information..." are a good place to begin, but there are many other companies to contact. Another place to collect information is on Compuserve. If you type "GO Plugplay" at the main system prompt, you will enter the Plug-and-Play forum, which contains many specifications and correspondence. If

you post messages in this forum, you will probably receive replies from the most knowledgeable people in the PnP community.

My experience with GO Plugplay wasn't entirely satisfactory, however. Although I successfully downloaded and unZIPped (decompressed) a file that purportedly contains a specification, none of our word processors could recognize the format. A look into the file with a utility program revealed a line near the beginning containing the phrase "Microsoft Word for Windows 6.0." Presumably, that word processor was used to create the file, so I don't understand why our word processors can't open the document when they can read files from Word for Windows V6.0.

Another source of help is the Plug-and-Play Association (PnPA). Contact information for this group appears in the **box**, "For free information...." PnPA holds semiannual "PlugFests." These meetings are not trade shows and are not open to the public, but they are open to product developers by invitation. PnPA developed the PlugFest concept because requests from developers to verify products' PnP compatibility were swamping the interoperability labs at Intel and Microsoft. The two companies have developed a suite of tests that products must pass before their vendors can label them with the Windows 95 logo. Developers who bring a product to a PlugFest can perform compatibility tests there.

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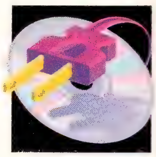
References



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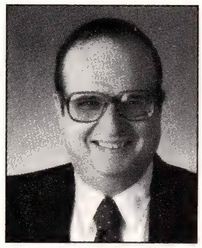

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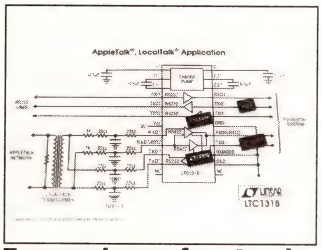
Line-interface unit provides dual T1/E1 transceivers on a single chip. The LXT332 has a digital jitter attenuator, switchable to either the transmit or receive side that eliminates the need for external crystals. The chip also integrates network-maintenance features such as a QRSS generator and detector to help reduce system cost. In a 44-pin PLCC, $29 (1000). **Level One Communications Inc**, Sacramento, CA. (916) 855-5000. **Circle No. 534**



Transceivers for AppleTalk and LocalTalk applications run from single 5V supply. The LTC1318 implements AppleTalk or LocalTalk on data-communication equipment, the peripheral side of a communication link. The LTC1323 is for data-terminal equipment, the computer side of a communication link. Powered by a single 5V supply, the chips use charge pumps and external capacitors to create other required voltage levels. The driver outputs and receiver inputs are protected against 10-kV ESD strikes. The LTC1318, in a 24-pin plastic DIP, costs from $3.65; the LTC1323, in a 16-pin plastic DIP, starts at $4.30. **Linear Technology Corp**, Milpitas, CA. (408) 432-1900. **Circle No. 535**

RS-485/RS-422 transceiver has high input impedance, allowing 128 transceivers on the bus. The MAX1487 features reduced-slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 2.5 Mbps. The device draws 230-μA quiescent current. From $1.25. **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600, ext 6087. **Circle No. 536**

Chip set performs MPEG-2 audio encoding and decoding. Musicore v.1.1 implements real-time digital compression and decompression of audio using MPEG-2 subsample rates. The chip set lets you take advantage of subsample rates and lower bit rates to save transmission-channel space and reduce storage requirements. It provides MPEG-2 sample rates of 16, 22.05, and 24 kHz at bit rates of 8, 16, and 24 kbps. The chip set comprises a 64k×8-bit boot ROM and an 8XC51-type microcontroller containing the Musicore management program. The device requires a DSP56002-type device and three 32k×8-bit SRAMs to operate. Sample price is $400, and production quantities sell for $125 (500). **Philips Semiconductors**, Sunnyvale, CA. (800) 234-7381. **Circle No. 537**

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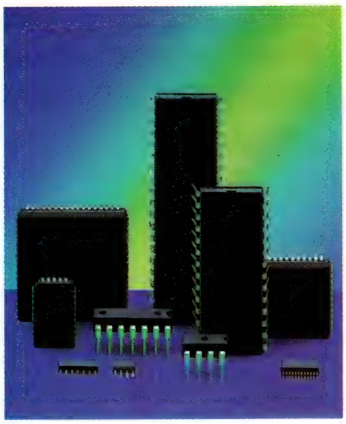

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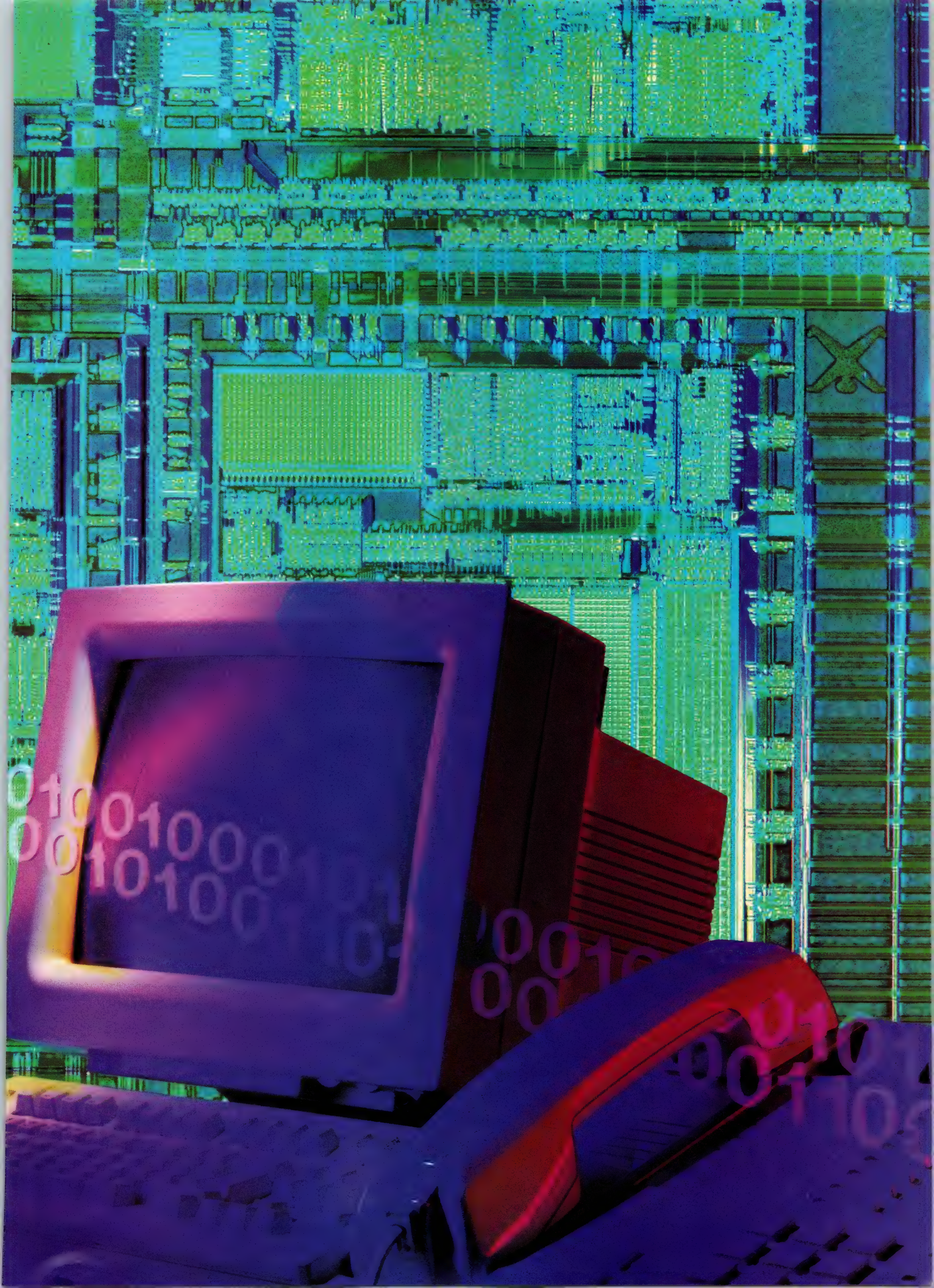


relay performs the switch-hook function in fax/modem applications. Prices range from \$0.63 to \$2.68 (10,000). **Siemens Components Inc**, Cupertino, CA. (408) 257-7910.

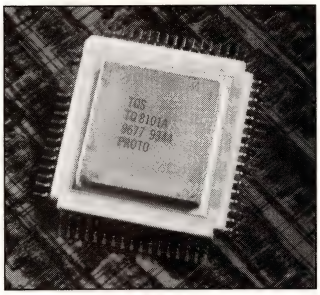
Circle No. 538

Real-time MPEG 2 video encoder suits digital TV. The CLM4700 MPEG 2 video-encoder family combines the company's Video-RISC processors with one of several microapplications programs to support main-level, main-profile, or frame-based encoding in various video formats. Compressed digital video lets you store video on random-access media and transmit as many as 10 digital video programs in place of one analog video program. The CLM4700 main-level, main-profile encoder costs \$12,000. The CLM47050 frame-based encoder costs \$8000. **C-Cube Microsystems**, Milpitas, CA. (408) 944-6300.

Circle No. 539

Quad DS1/E1 line transceiver suits telecommunications. The T7693 offers four fully independent transceivers under the control of a shared high-speed μP interface. Each channel operates at 1.544-Mbps DS1 or 2.048-Mbps CCITT E1 operation. The chip integrates all transmit, receive, equalization, clock recovery, and jitter- attenuation functions; the device integrates all output drivers, oscillators, and PLLs on chip. The 100-pin fine-pitch PQFP dissipates 110 mW/channel. \$39.95 (10,000). **AT&T Microelectronics**, Allentown, PA. (610) 712-4106.

Circle No. 540



SONET- and SDH-compatible 622-Mbps interface IC chip set. The TQ8101/TQ8103 chip set provides functional integration for SONET (OC-12) and SDH (STM) interface applications and meets the Bellcore jitter performance specification. The chips provide multiplexing, demultiplexing framing, clock-synthesis PLL, loopback, and clock-data-recovery functions. TQ8101, \$139; TQ8103, \$83 (1000). **Triquint Semiconductor Inc**, Beaverton, OR. (503) 644-3535. **Circle No. 541**

Dual JFET-input comparator has 1.5-nsec propagation delay. The SPT9693 has JFET inputs that reduce input-bias currents to nanoamp levels, eliminating the need for input drivers and buffers in most applications. The comparator has a common-mode input voltage range of –3 to +8V, a tracking bandwidth of 300 MHz at –3 dB, an open-loop gain of 60 dB, and an input capacitance of 1 pF. Complementary outputs compatible with ECL levels drive 50Ω loads. From \$19.50 (1000). **Signal Processing Technologies Inc**, Colorado Springs, CO. (719) 528-2300.

Circle No. 542

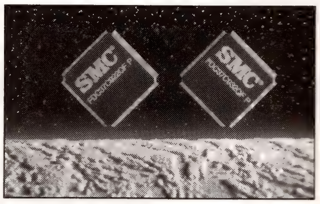
FPGAs comply with PCI. The XC3100A field-programmable gate-array (FPGA) family complies with the Peripheral Component

Interconnect (PCI) bus specification, a fundamental building block in many high-performance PCs and workstations. The family comprises five devices with 1500 to 7500 usable gates and with prices starting at $34. A hard-wired version, the XC3400, starts at $7.90. **Xilinx Inc**, San Jose, CA. (408) 559-7778.

Circle No. 543

14-bit 1-MHz analog processor for CCDs improves system performance under low-light conditions. The ET4261 offers a differential-input signal conditioner, lowpass filter, correlated double sampler, difference amplifier, and low-noise 14-bit A/D converter. The device dissipates 2.2W. It comes in a 2.5×2.5×0.4-in. package and costs $446 (100). **Edge Technology Inc**, Waltham, MA. (617) 899-7900.

Circle No. 544



Parallel-port floppy-disk controller also offers keyboard controller and real-time clock. The FDC37C922 ($12 (10,000)) includes a floppy-disk controller with data rates to 2 Mbps, a digital-data separator, an IDE interface, a high-speed parallel port with a 16-byte FIFO buffer, and two high-speed NS16C550-compatible UARTs. The chip also has an enhanced 8042 software-compatible keyboard controller with 2 kbytes of BIOS ROM, an MC146818/DS1287-compatible real-time clock, and a mouse port. In power-down mode, the chip draws 500 nA. The FDC37C932 ($13 (10,000)) adds compatibility with Microsoft's Windows 95 and Version 1.0a of the ISA Plug-and-Play standard. The chip has an EEPROM interface and 14 multifunction I/O pins to which the system processor can assign functions. **Standard Microsystems Corp**, Hauppauge, NY. (516) 273-3100.

Circle No. 545

14-bit ADC converts at 20M samples/sec. The ADC3120 hybrid sampling A/D converter provides 14-bit accuracy with a 90-dB spurious-free dynamic range, 85-dB THD, and a 75-dB S/N ratio. The ECL-compatible device comes in a 1.6×2.4×-0.225-in. metal package and dissipates 4W. $3500. **Analogic Corp**, Peabody, MA. (508) 977-3000.

Circle No. 546

Graphics processor handles 300,000 shaded, depth-buffered, and antialiased polygons/sec. This chip lets Pentium-based PCs with the Glint 300SX 3-D processor outperform workstations when running OpenGL applications, according to the manufacturer. The chip provides 32-bit color, 2- and 3-D acceleration, an on-chip Peripheral Component Interconnect-compliant local-bus interface, and an integrated look-up table/DAC control. The chip contains >1 million transistors and implements all 3-D rendering operations of OpenGL in hardware, including Gouraud shading,

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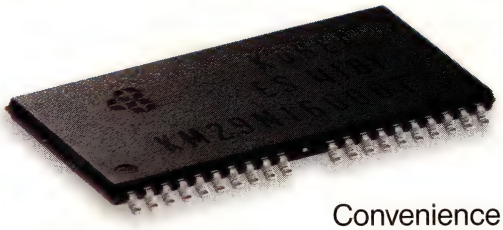

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SRAM (SYNCHRON)	288 K/1-2 M	x9, x18, x32, x36, x64	80/100 MHz	SOJ, PLOC, PQFP, BGA
SRAM (LOW POWER)	64 K–4 M	x8	45–120	DIP, SOP, TSOP, SDIP
PSEUDO SRAM	1 M	x8	80–120	DIP, SOP, TSOP, SDIP
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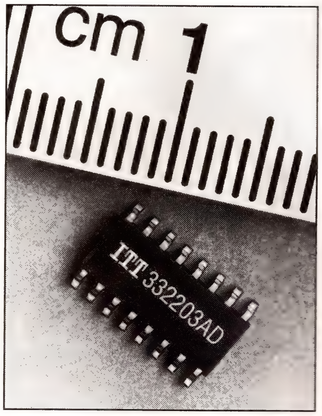
depth buffering, antialiasing, and texture mapping. $150. **3Dlabs Inc**, San Jose, CA. (408) 436-3455.

Circle No. 547

Battery-backed RAM and clock RAM have 10-year battery pack. The M48Z58/59 is a low-power, 8k×8-bit CMOS SRAM, power-fail-control circuit, and battery in a single package. The power-fail-control circuit monitors the V_{CC} line and switches to battery power whenever the voltage level is out of tolerance. The M48T58 also includes a quartz crystal and a real-time clock/calendar circuit. The M48T59 adds a programmable alarm and a programmable watchdog timer. The devices are available in both through-hole and surface-mount packages. Prices range from $4.50 to $9 (10,000). **SGS-Thomson Microelectronics**, Lincoln, MA. (617) 259-0300.

Circle No. 548



RF power amplifier suits wireless communications. The ITT332203AD two-stage RF power amplifier operates in the 1800- to 1900-MHz frequency band for digital European cordless telephones (DECTs) and personal-communications systems. The amplifier has an output power of 400 mW, meeting the requirements for DECT equipment with 2 to 3 dB of path loss between the power amplifier and the antenna. The device has a 28-dB power gain and a 370-mA typ current consumption when driven to full output. The device operates from a 3.6V battery and requires no negative power source. Available in a 16-pin narrow body SOIC, the amplifier costs $5 (1000). **ITT GTC**, Roanoke, VA. (703) 563-8600.

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64-macrocell PLD has 10-nsec propagation delay and 100% routable interconnects. The CY7C372 has 32 I/O pins and comes in 44-pin PLCC and CLCC packages. From $9.85(1000). The CY7C373 offers 64 I/O pins in 84-pin PLCC and CLCC packages or a 100-pin TQFP package. From $12.60. **Cypress Semiconductor**, San Jose, CA. (408) 943-2600.

Circle No. 550

16-kbit serial EEPROM includes 16-byte OTP security block. The 24LC174 provides the one-time-programmable (OTP) security block for wireless communications products and others that need to prevent tampering with identification codes. The device operates from 2.5 to 5.5V with a standby current of 5 to 10 µA. Typical active current is 1 mA. The device comes in eight-pin DIP and SOIC packages and costs $2.41 (1000). **Microchip Technology Inc**, Chandler, AZ. (602) 786-7200.

Circle No. 551

SMART-BATTERY TECHNOLOGY: POWER MANAGEMENT'S MISSING LINK

You no longer need to view a battery as a power-generating element whose characteristics are beyond your knowledge and control. The technology now exists to provide batteries with varying degrees of smarts, forming a critical link between the battery and host equipment.

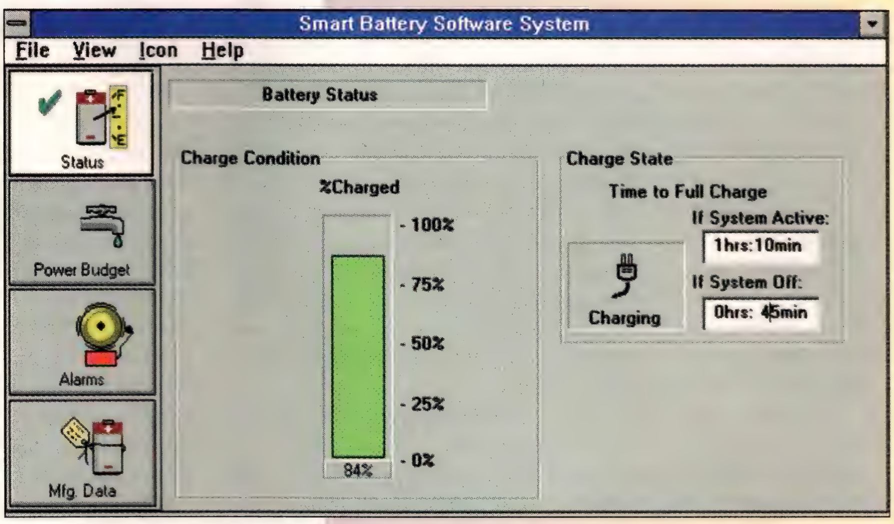
ANNE WATSON SWAGER, TECHNICAL EDITOR

A smart-battery-management philosophy and a surge of battery-management products now provide you with powerful means to optimize battery performance. Smart-battery technology produces accurate information about the state of a battery and enables optimum charge control. One implementation of this technology is a standardized smart battery that includes all the necessary electronics to monitor itself and communicate to its host (see **box** on pg 50, "What's a smart battery?"). However, you can also team up many available ICs and batteries to tailor the battery's level of intelligence to your particular system.

The need for smart-battery technology stems from the introduction of new battery types, each with its own stringent requirements for charging. In many cases, battery manufacturers won't supply these batteries—nickel-metal hydride (NiMH) and lithium-ion (Li-ion) batteries in particular—without mandating the use of an approved charge-control scheme.

NiMH batteries are more sensitive to overcharge than their NiCd relations. High heat resulting from a high-rate overcharge is most damaging to an NiMH battery's capacity and cycle life. Thus, fast charging an NiMH battery requires tight control of charging characteristics and accurate feedback about the state of the battery.

Although not widely available, Li-ion batteries mandate tight battery management for safety purposes alone. Li-ion batteries are simply dangerous if not charged properly. As one manufacturer said, "without battery management, Li-ion batteries wouldn't exist in the marketplace."



One goal of an intelligent battery and battery-management system, which this example GUI illustrates, is to provide reliable data—charge condition and charge state—to the end user. Another important goal is to control charging to enhance battery life. (Courtesy of SystemSoft Corp)

The concept and underlying technology of a smart battery is not new. In 1989, without much fanfare, Sanyo Energy USA introduced the SI101, a fast-charge control module for NiCd and NiMH batteries ($6.89 for 10,000 of the modules, $2.93 for just the IC). The company has integrated the module into battery packs for a wide variety of OEM customers. Many top-tier computer manufacturers are on this list, and others have developed their own battery-management schemes and ICs.

However, recent industry developments have put the spotlight on smart batteries and battery management. In an effort to standardize smart batteries and the way they communicate, Duracell and Intel introduced the System-Management Bus and Smart-Battery Data Specification last year. They hope their efforts, which included widespread industry input, will lead to a standard power-management bus for portable equipment and a standard smart-battery hardware configuration and data set (see **box**, "Smart-Battery and System-Management Bus Specifications"). The standards push is not without controversy (see **box**, "The debate over smart-battery standards," pg 59).

This year, Duracell will introduce its smart-rechargeable batteries as the first products to comply with these specs. However, many companies have designed intelligent-battery schemes of their own and perfected the underlying technology necessary to bestow battery

SMART-BATTERY AND SYSTEM-MANAGEMENT BUS SPECIFICATIONS

The Smart-Battery Specification jointly developed by Intel and Duracell—with input and feedback from major computer OEMs and component suppliers—attempts to address the three major problems that batteries pose to equipment designers and end users. Batteries are unpredictable and, in their simplest form, have no knowledge of remaining operating time. Battery-powered equipment has difficulty determining if the battery can supply power for an additional load. And, you must tailor current battery chargers to a specific battery chemistry.

The ultimate smart battery would provide complete information on its state of charge; answer questions of remaining capacity, based on a certain discharge rate; control its own charge regime that may vary with battery chemistry; and provide information on its history, such as maximum temperature extremes and numbers of cycles.

The Duracell/Intel specification attempts to provide this information according to each company's interests in the battery and portable-equipment marketplace. Duracell's interest in developing this specification is to standardize all types of rechargeable batteries. Intel's interest is to further the acceptance of its power-management bus, which they hope would further the use of portable computers. Although the companies tightly aimed the specification at the portable-computer industry, it is applicable to other portable products. Remember that the well-thought-out scheme they present is only one way to implement an intelligent battery system.

The specification itself comprises two essential parts: one defines a two-wire power-management bus that can communicate with various components, including but not limited to batteries. Intel's Architecture Labs created this System-Management Bus, or SMBus. The second is the actual smart-battery data and charger specification that details the batteries' data set and charge-control schemes.

The bidirectional SMBus lets you send any type of command with two wires that link all components. The bus's goal is to improve mobile systems by enabling better power-management software and hardware and providing more control over power-managed components. The SMBus uses the I²C-bus as its backbone and adds a software protocol (a definition of bus transfers, commands, etc) on top of I²C's physical electrical layer. The SMBus specifies certain voltages, such as logic-0 and -1 threshold voltages, more tightly.

The SMBus has much in common with the Access.bus protocol because both are based on I²C. The manufacturer intended the SMBus to act as an internal bus for connecting nonremovable components (the battery is the only exception). The Access.bus is an external bus for Plug-and-Play capability for external peripheral devices. However, the Access.bus spec can accommodate SMBus devices. Thus, a single controller can handle both.

The Smart-Battery Data Set

The Smart-Battery Specification defines a smart battery as "a battery equipped with specialized hardware that provides present state, calculated, and predicted information to its SMBus host under software control." The Smart-Battery Data (SBD) specification defines the data that flows across the SMBus between a smart battery, SMBus host, smart-battery charger, and other devices. The SBD specification includes software definition, error-detection, and signaling; the smart-battery data protocols; and the smart-battery data set of all messages between the host, smart battery, and smart-battery charger.

The data set defines 34 values of battery information. These values include temperature, voltage, and current. The data set also includes computed and stored values, such as AtRateTimeToEmpty (the predicted remaining operating time if the battery is discharged at the AtRate), RunTimeToEmpty (the predicted remaining battery life at the present rate of discharge), AverageTimeToEmpty (a one-minute rolling average of the predicted remaining battery life), AverageTimeToFull (a one-minute rolling average of predicted time until the battery reaches full charge), RemainingCapacity (in units of either current or power), RelativeStateOfCharge (predicted remaining capacity as percent of full-charge capacity), FullChargeCapacity (predicted pack capacity when fully charged), and CycleCount (number of charge/discharge cycles of the battery).

Fig A shows a possible smart-battery implementation that consists of a single battery (the spec also allows extensions for multiple batteries), battery charger, and a host. As envisioned in the specification, the smart charger is independent of the

intelligence, such as gas-gauge and charge-control techniques (see **box**, "For free information..." pg 63). Since 1991, Benchmarq Microelectronics has designed six gas-gauge ICs. In addition to Sanyo's module, Energizer Power Systems and National Semiconductor have teamed to develop an intelligent-battery chip set. And Rayovac and Benchmarq Microelectronics have cooperated on the design of an IC to control charging of Rayovac's Renewal line of reusable alkaline batteries. Rayovac plans to offer a full rechargeable system comprising four AA cells, the bq2901 IC, and a wall-cube adaptor for an OEM price of less than $6.

Finally, software vendors are getting involved. SystemSoft and Phoenix Technologies offer software that makes some of the battery data that an intelligent battery supplies available to a computer end user. The goal of such products is to let the user make changes in power-management software. The software would indicate what affect these changes would have on battery capacity.

The advantages of a high IQ

The advantages of an intelligent battery or intelligent battery-management system are clear: longer run times, longer lifetimes, and more end-user confidence in the battery information. Batteries that can deliver accurate information about their state of charge let you use all of that available charge more fully. Shorter charge times, which must

battery, but under the battery's control. Also, to be compatible with multiple battery chemistries, the battery must have some control of the charge regime. Chargers that closely cooperate with the battery have two distinct advantages. First, they provide the battery with all the power it can handle without overcharging, and second, they can recognize and correctly charge batteries with different chemistries and voltages.

Smart-battery chargers

The smarts in a battery are basically for self-monitoring and communication. For controlled charging, the battery needs a smart charger listening to it. The battery knows how it must be charged, but the actual power generation is the job of the external charger. According to the specification, a smart-battery charger is "a battery charger that periodically communicates with a smart battery and alters its charging characteristics in response to information provided by the smart battery."

At the very least, a smart battery has a charge-control algorithm, but a smart charger can also have algorithms. You can implement a simple system, one in which the battery simply communicates whether it wants to be turned on or off. Or, you can implement a more sophisticated system, one in which a charger is smart enough to control a specialized battery.

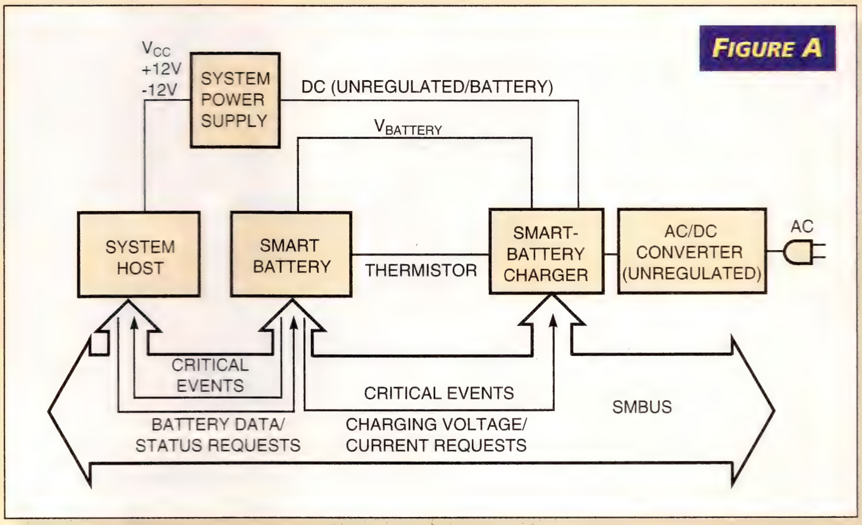
To accommodate these possible schemes, the Smart-Battery Charger Specification defines three levels of chargers. Level-1 chargers can only interpret the battery's critical warning messages that indicate the system should no longer charge a battery. A level-1 charger can't adjust its output in response to requests from the battery or host, thus, it is *not* chemistry independent.

In addition to supporting level-1 commands, a level-2 charger is an SMBus slave device that responds to charging voltage and current messages sent from the smart battery and can dynamically adjust its output characteristics. Using the charging algorithm in the battery, the level 2-charger may simply set a charge condition once or may adjust its output periodically to meet the needs of the changing battery. Thus, a level-2 charger is chemistry independent.

A level-3 charger is an SMBus master device. This charger can poll the battery to determine the battery's desired charging voltage and current and can dynamically adjust its output to meet the battery's charging requirements. In addition to all capabilities of a level-2 charger, a level-3 charger can also implement an alternative specialized charging algorithm and can interrogate the battery for any relevant data, such as time remaining to full charge, battery temperature, or other data used to control proper charging and discharging.

To order a copy of the Smart-Battery and SMBus specification, call (503) 797-4216 or (800) 253-3696, or e-mail ial_product@ccm.hf.intel.com and specify product code SBS5220.

FIGURE A



As envisioned by Duracell and Intel in their Smart-Battery Specification, a typical single smart-battery system consists of a power supply, host, smart battery, and smart-battery charger. The last three communicate via the two-wire serial SMBus.

be commensurate with controlled charging, result in longer run times. And, proper handling of the battery results in the longest possible life for that battery.

Depending on the specific implementation, other advantages include a management scheme that can recognize and handle batteries of different chemistries. The Duracell/Intel spec and many of the battery-management products can currently deal with numerous battery chemistries, including NiCd, NiMH, Li-ion, and lead acid. In addition, many ICs tailored specifically for Li-ion batteries will appear this year.

One of the greatest advantages of smart batteries or systems is the power-management possibilities they offer to a system engineer. These batteries provide a wealth of information that you can use to develop a proprietary power-management scheme, regardless of whether you use a standard battery or communication protocol. Dave Heacock of Benchmarq Microelectronics suggests adaptive charge control as one such technique. Using information from an intelligent battery, you could design a system that caters its sensitivity to the reported battery state. If you know a battery is empty, you could design the system to apply the full charge current. Once the battery fills up, the system could increase the sensitivity to identify the end-of-charge point very closely.

WHAT'S A SMART BATTERY?

There is no standard definition of a "smart" battery. Duracell defines a smart battery as "a rechargeable battery equipped with a microchip that collects and communicates present, calculated, and predicted battery information to the host system—notebook computer, cellular phone, etc—under software control."

Aside from this definition that implies a hardware configuration, there is a general consensus on at least some of the qualifying features of an intelligent battery and associated battery-management systems. These features can include the battery performing accurate self-monitoring; implementing its charge-regime control; communicating with its host; implementing fault identification/protection; and storing pertinent information, including its charge/discharge cycle history.

This list of intelligent-battery features may seem to imply that the intelligence has to reside in the battery pack, but this is not always true. In some cases, separate circuits make more sense.

Smart-battery qualities

In some cases, a truly self-contained smart battery may be the right choice for your product. However, you have other choices. Although the Duracell/Intel specification's goal is standardization, the spec has flexibility and contains many implementation layers from which you can pick and choose. For example, a high-end computer may include all smart-battery electronics in the battery pack, but the same computer manufacturer could also produce a cheaper line with a slightly modified battery pack.

While standardization is under debate, you can choose how much intelligence to design in and where to locate it (see **box**, "Looking ahead," pg 59). A certain level of intelligence may suit one product but be overkill for another. The requirements of the notebook-computer user differs greatly from the occasional cellular-phone user, for example.

Duracell's first products to meet the Duracell/Intel Smart-Battery Specification, the Smart Rechargeable Batteries, indicate remaining capacity and run time within an estimated 1%. The batteries have an on-pack LED that indicates remaining battery life in increments of 25%.

Obviously, much of what you design depends on the product's battery chemistry or on the desire to handle multiple chemistries. Remember: Every battery has a unique personality profile (see **Ref 1**). Battery characteristics change over time (self-discharge), with temperature, and with use and abuse. The battery type can experience varying degrees of these changes, and you have to account for these changes when choosing a battery-management scheme.

The complexity of the control schemes may impact your battery choice. For any product, the advantages of NiMH or even Li-ion batteries may not outweigh the costs of controlling them. Rayovac's Renewal alkaline batteries—which are suited more for low-power, hand-held devices than for notebook computers—have very low self-discharge rates, so predicting remaining charge doesn't require as sophisticated a monitoring scheme as NiCd or NiMH batteries. An interesting feature of the Renewal battery is a mechanical interlock that allows a sys-

SMART-BATTERY TECHNOLOGY

tem to charge only the Renewal battery while running on another battery of a different chemistry.

Currently, you can implement either a full-blown smart battery or an intermediate level of battery management in three ways: You can use a fully integrated, retail smart battery, such as the DR15, 17, 30, 35, and 36 from Duracell. You can work with a manufacturer, such as Energizer Power Systems or Sanyo Energy, on a unique design based on a fully integrated smart battery. Or, you can mix and match products from companies that design battery-management and charge-control ICs, microcontrollers, and software.

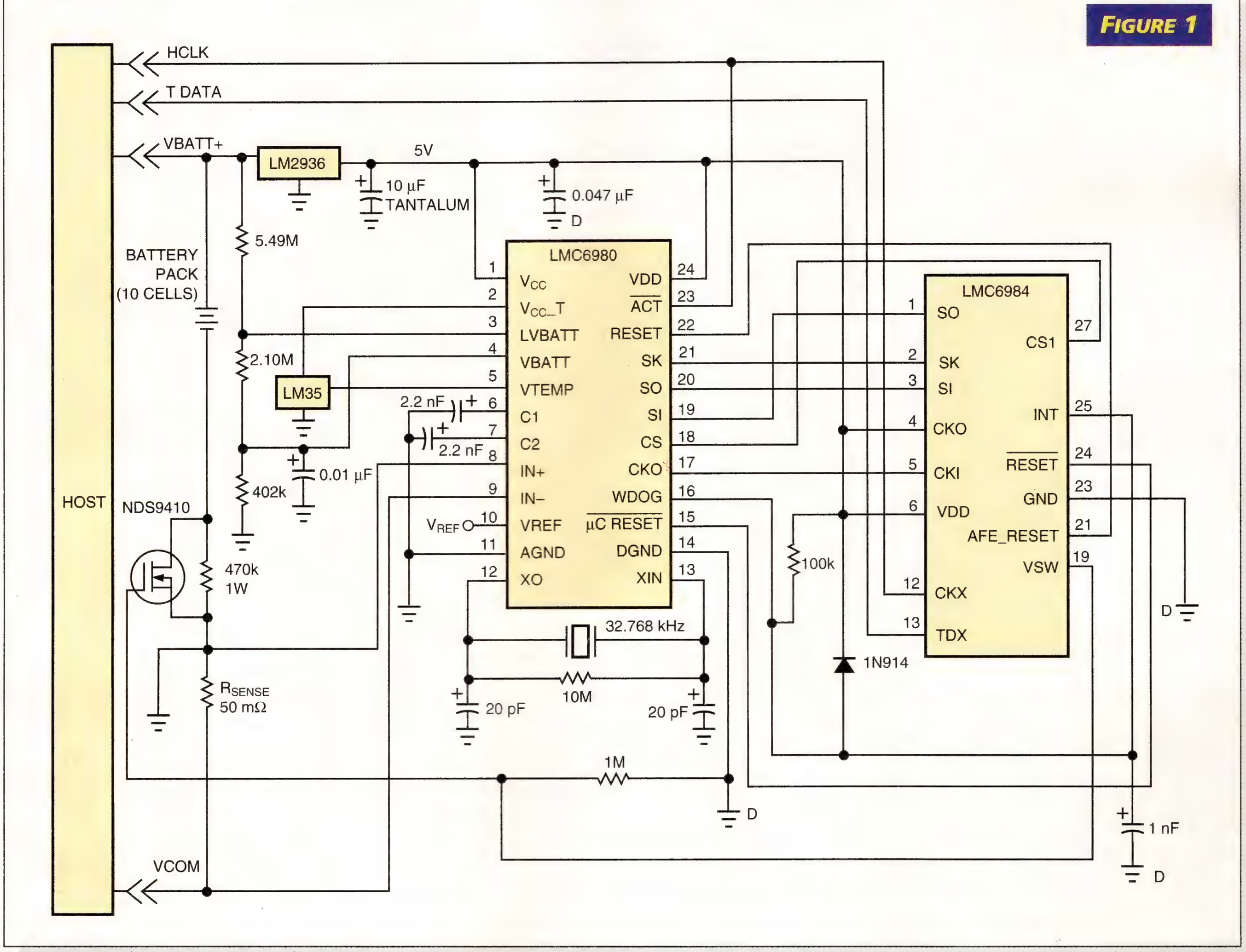
Duracell's batteries epitomize the use of a fully integrated, retail smart battery. The company's smart batteries conform to one of five form factors with varying levels of capacity.

Products from Energizer Power Systems and Sanyo Energy epitomize the second approach. The companies have more or less a custom working relationship with OEM customers and offer design flexibility for the electronic design and hardware form factor. For example, when working with Energizer Power Systems, you can implement any proprietary bus system and battery-data set, or you can actually emulate elements of the Duracell/Intel Smart-Battery and SMBus specification.

Energizer Power Systems worked with National Semiconductor for the design of the actual silicon, which works with a variety of manufacturers' batteries and, thus, suits the final mix-and-match option. The chip set ($8 to $10 for the highest end) consists of the LMC6980 intelligent-battery development system and the LMC6984 intelligent-battery embedded controller (**Fig 1** shows a typical application circuit).

The LMC6980 contains the analog data-acquisition circuitry to monitor the battery's voltage, temperature, and dynamic current. The IC is unique because it contains 128 bytes of internal embedded EEPROM for storing numerous battery and charge-termination

FIGURE 1



The LMC6980 and LMC6984 chip set from National Semiconductor, along with some external components, such as the LM2936 low-dropout regulator and LM35 temperature sensor, implement an intelligent-battery charge-control system. The LMC6980 performs data-acquisition functions and contains internal EEPROM; the LMC6984 contains charge-control firmware.

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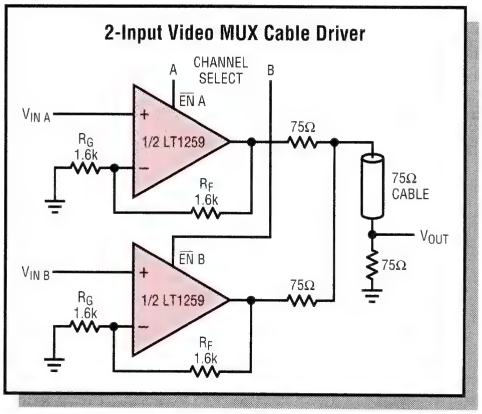
Dual and Triple 130MHz Current Feedback Amplifiers Have Individual Shutdown Pins for MUX Applications

The dual LT1259 and the triple LT1260 are 130MHz, 1600V/µs current feedback amplifiers with individual shutdown pins. Not only does the shutdown function reduce the supply current to 0mA, but it puts the outputs into a high impedance state, ideal for multiplexing.

Other key features include:
- 0.1dB gain flatness > 30MHz
- Supply current: 5mA per amp
- Fast shutdown: 40ns turn-off time; 100ns turn-on time
- Output current: 60mA
- Differential gain: 0.016%
- Differential phase: 0.075°
- Supply voltage range: ±2V (4V) up to ±15V (30V)



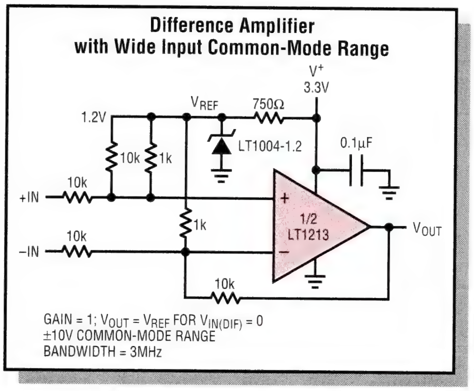
Three amplifiers in one package optimizes the LT1260 for amplifying RGB or YUV signals for video and graphics. Fast switching times make it ideal for MUXing in multimedia applications. The LT1259/60's 0.1dB gain flatness beyond 30MHz will appeal to HDTV system designers.

The LT1259 is offered in 14-pin DIP and SOIC, the LT1260 comes in 16-pin DIP and SOIC. 1000-piece pricing for the LT1259 and LT1260 starts at $3.31.

Single Supply Dual Op Amp Offers DC Precision and Fast AC Performance

The LT1213 dual op amp sets new standards in single supply op amp performance. Wideband capability and DC precision are no longer mutually exclusive. This enables the LT1213 to perform in applications ranging from high speed photodiode amplifiers to 12-bit accurate DAC current-to-voltage converters.

Key LT1213 features include:
- Gain-bandwidth product: 28MHz
- Slew rate: 12V/µs
- 0.01% settling time (10V step): 1.1µs
- Maximum input offset voltage: 275µV
- Maximum drift: 6µV/°C
- Minimum open-loop gain: 121dB
- Maximum input bias current: 200nA
- Maximum input offset current: 40nA
- Low noise: 10nV/$\sqrt{\text{Hz}}$
- Supply current: 2.7mA per amp
- Output current: 50mA
- Fully specified at 3.3V, 5V and ±15V



The LT1213 can drive up to 1000pF of load capacitance, ideal for active filters and buffers. An A-grade is offered for the dual LT1213. A quad version, the LT1214, is also available. For other devices in the family, see the table below.

The LT1213 is available in 8-pin PDIP and SOIC and starts at $3.30 in 1000-piece quantities.

LT1211-16 Family of Single Supply, High Speed Precision Amplifiers

Dual	Quad	I_{SUPPLY} per Amp	GBW	Slew Rate	Max V_{OS}	Max I_B
LT1211	LT1212	1.3mA	14MHz	7V/µs	275µV	125nA
LT1213	LT1214	2.7mA	28MHz	12V/µs	275µV	200nA
LT1215	LT1216	4.8mA	23MHz	50V/µs	450µV	600nA

LINEAR TECHNOLOGY

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Milpitas, CA 95035-7487
Phone: (408) 432-1900
Fax: (408) 434-0507
For literature only: 1-800-4-LINEAR

LT/0295

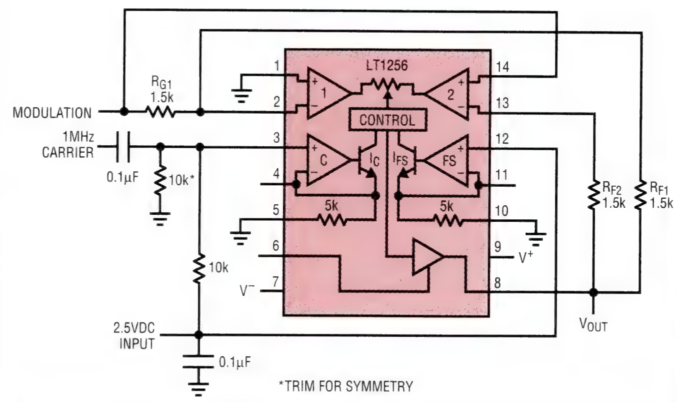
40MHz Video Amplifiers Implement Fader and DC Gain Control Functions

The LT1251 and LT1256 are two-input 40MHz, 300V/µs current feedback amplifiers with control circuitry that sets the amount of signal each input contributes to the output. The LT1251 is optimized for fader applications; the LT1256 is designed for DC gain control. Distortion is a low 0.01%.

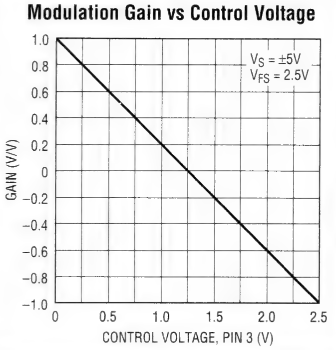
For control signals of less than 2%, or more than 98%, the LT1251 includes circuitry that sets one input completely off (0%) and the other completely on (100%). This eliminates control overdrive requirements in fader applications. The LT1256 doesn't have this feature and operates linearly over the entire control range. Gain accuracy is guaranteed better than ±3% over temperature. Differential gain and phase are a low 0.02% and 0.02°, ideal for composite video applications.

The LT1251/LT1256 draw only 13mA and have operating voltages from 5V up to ±15V. The devices are offered in 14-pin PDIP and 14-pin SOIC. 1000-piece pricing for the LT1251/LT1256 starts at $5.76.

Four-Quadrant Multiplier as a Double-Sideband Suppressed-Carrier Modulator



Modulation Gain vs Control Voltage



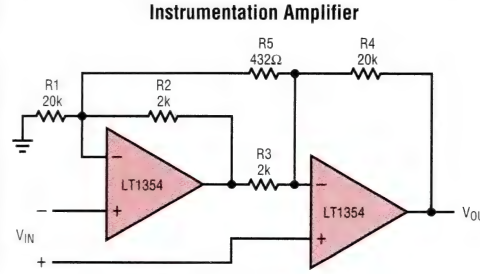
Low Power Op Amp Slews 400V/µs and Uses Only 1mA per Amplifier

The LT1354 is a low power, high speed voltage-mode op amp. The unity-gain stable LT1354 has a 12MHz gain-bandwidth product and a 400V/µs slew rate while drawing only 1mA. Settling time to 0.01% (10V step) is 280ns. Its minimum output current of 25mA can drive ±12.5V into 500Ω. The LT1354 is a C-Load op amp and can drive unlimited capacitive loads.

Because of its impressive AC specs, the LT1354's DC specifications tend to be overlooked. They shouldn't because they're equally impressive: 800µV maximum V_{OS}, 300nA maximum I_{BIAS}, 70nA maximum I_{OS}.

The balance of good ACs and DCs makes the LT1354 ideal for applications ranging from active filters and buffers to photodiode amplifiers and data acquisition systems. Operating supply range is from ±2.5V (5V) up to ±15V (30V).

Instrumentation Amplifier



$$A_V = \frac{R4}{R3}\left[1+\frac{1}{2}\left(\frac{R2}{R1}+\frac{R3}{R4}\right)+\frac{R2+R3}{R5}\right] = 104$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON-MODE REJECTION
BW = 120kHz

Dual and quad versions of the LT1354, the LT1355 and LT1356, are also available. For other members of this high speed, low power family, see the table below. 1000-piece pricing for the LT1354 starts at $2.24.

LT1354-65 Family of High Speed, C-Load Operational Amplifiers

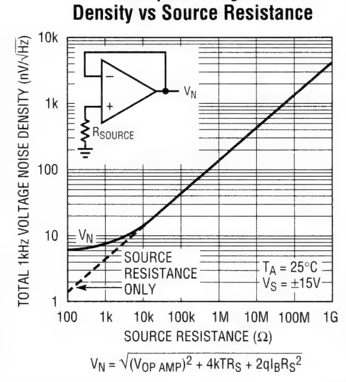
Single	Dual	Quad	I_{SUPPLY} per Amp	GBW	Slew Rate	Max V_{OS}
LT1354	LT1355	LT1356	1mA	12MHz	400V/µs	800µV
LT1357	LT1358	LT1359	2mA	25MHz	600V/µs	600µV
LT1360	LT1361	LT1362	4mA	50MHz	800V/µs	1mV
LT1363	LT1364	LT1365	6mA	70MHz	1000V/µs	1.5mV

FET-Input Dual Op Amp Offers Low Current *and* Voltage Noise

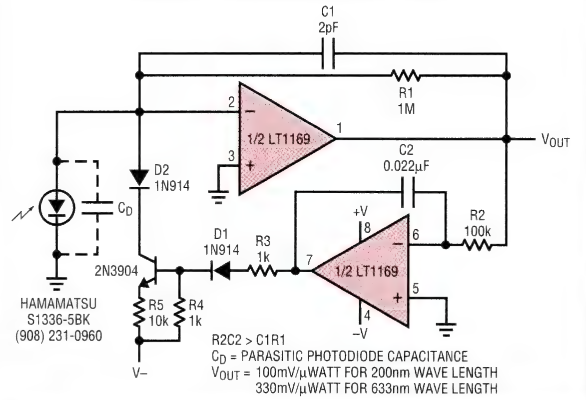
The LT1169 dual op amp not only provides the low input current noise of a JFET, it also has a guaranteed maximum input voltage noise of $8nV/\sqrt{Hz}$ at 1kHz ($6nV/\sqrt{Hz}$ typ). Guaranteed specifications are provided at ±5V and ±15V; voltage noise is 100% tested.

Other key features of the LT1169 include:
- Input current noise: $1fA/\sqrt{Hz}$
- **Input bias current: 5pA max over the entire input range**
- Input capacitance: 1.5pF
- Input offset voltage: 2.0mV max
- Voltage gain: 1.2V/μV min
- Supply current: 5.3mA per amp
- Gain-bandwidth: 5.3MHz

1kHz Output Voltage Noise Density vs Source Resistance



Low Noise Light Sensor with DC Servo



The LT1169's low current *and* voltage noise make it an ideal building block for photocurrent amplifiers, hydrophone amplifiers and low noise instrumentation amplifier front ends. For an even lower input voltage noise, FET-input amplifier, look at the LT1113 dual op amp.

For lower input bias current and offset voltage, an A-grade version of the LT1169 is offered. Pricing for the LT1169 starts at $3.80 in 1000-piece quantities.

Rail-to-Rail Input, Rail-to-Rail Output, Zero-Drift Op Amp Operates Down to 3V and Drives Capacitive Loads

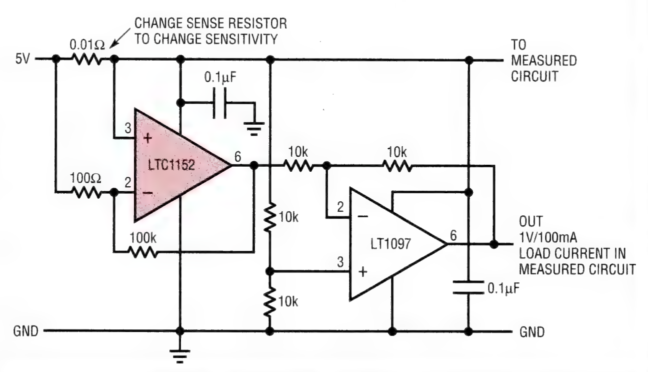
The LTC1152 zero-drift, C-Load op amp includes several features: an input common-mode range that includes both supply rails; an output that swings to the same rails; a power saving shutdown function; and finally, a compensation pin that enables the output to drive *any* capacitive load without oscillation. This last feature is especially useful for driving A/D converters or for interfacing with sensors and transducers.

The LTC1152's rail-to-rail capability makes it ideal for supply current sensing and for low voltage precision applications. The shutdown function drops the supply current to 1μA and puts the output into a high impedance state for easy multiplexing.

Additional LTC1152 features include:
- Input offset voltage: 10μV max
- Input offset drift: 100nV/°C max
- Input bias current: 10pA
- Open-loop gain: 130dB
- Minimum CMRR: 115dB
- Supply current: 2.2mA
- Supply voltage range: 2.7V to 14V
- Specified for 3V and 5V operation

Offered in 8-pin DIP and 8-pin SOIC, the LTC1152 starts at only $3.12 in 1000s.

High-Side Current Sensing Amplifier



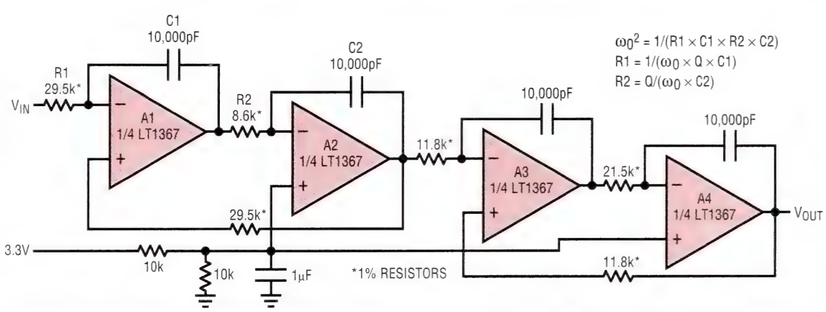
LINEAR TECHNOLOGY

Linear Solutions
Operational Amplifiers

Quad Precision Op Amp Has Rail-to-Rail Inputs and Outputs

The LT1367 is a quad precision op amp that has rail-to-rail capability on both input *and* output. Rail-to-rail capability is ideal for applications such as low voltage signal processing and supply current sensing.

Single 3.3V Supply 4-Pole State Variable Filter Using the LT1367



Precision DC specifications include a V_{OS} of 150µV and I_B of 10nA. I_{OS} is a low 6nA. A_{VOL} driving a 10kΩ load is 2 million. CMRR is 90dB over the entire rail-to-rail input range.

Operating voltage is as low as 1.8V and the device is fully specified for 3V, 5V and ±15V operation. Supply current is only 375µA per amplifier and output drive is 30mA.

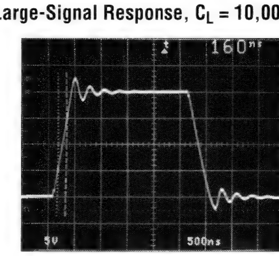
A dual version, the LT1366, is also available. The LT1366 and LT1367 are stable while driving capacitive loads up to 1000pF. The LT1368 and LT1369 are C-Load™ versions of the LT1366/LT1367 and drive loads of 10,000pF or more.

The LT1367 is offered in 16-pin narrow SOIC. Pricing for the LT1367 begins at $5.86 in 1000-piece quantities.

C-Load is a trademark of Linear Technology Corporation.

250mA Output, 60MHz Current Feedback Amplifier Serves HDSL and Video Distribution Applications

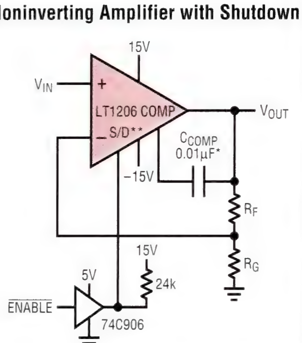
Large-Signal Response, C_L = 10,000pF



$V_S = \pm 15V$, $R_L = \infty$, $R_F = R_G = 3k$

The LT1206 is a 60MHz, 900V/µs current feedback amplifier with 250mA minimum output current. Its high output current and low distortion make it ideal for driving transformers in HDSL transceivers. Used for video distribution (Differential Gain: 0.02%, Differential Phase: 0.17°), the device easily drives 15 doubly-terminated 75Ω loads. By using the COMP pin, the LT1206 C-Load op amp is stable while driving capacitive loads up to 10,000pF and can easily supply the large currents required to slew these loads, a key requirement for pin drivers in ATE designs.

Noninverting Amplifier with Shutdown



*OPTIONAL, USE WITH CAPACITIVE LOADS
**GROUND SHUTDOWN PIN FOR NORMAL OPERATION

A SHUTDOWN feature switches the device into a high impedance, low power dissipation mode (I_S < 200µA). For lower bandwidth applications, the supply current can be reduced with a single external resistor. The LT1206 operates with supply voltages from ±5V to ±15V.

The LT1206 is available in 8-pin DIP, 7-lead TO-220, 7-lead DD and 8-pin SOIC packages. Pricing for the LT1206 in 1000-piece quantities begins at $3.30.

parameters. The LMC6984 contains all of the charge-control functions implemented by one of two versions of firmware. One is standard µC code. The other, which the company calls NeuFuz, is code the company derived using neural fuzzy-logic algorithms. The fuzzy-logic charge-control algorithms implement a charge time much faster than the typical two to three hours. Tests performed on NiCd batteries show charge times of around 20 to 30 minutes.

Other products that implement the mix-and-match approach are either complete battery-management ICs that you team with a selected battery, such as Benchmarq's bq2040 ($7 (1000)) and Microchip Technology's MTA-11200 ($3.75 (10,000)), or stand-alone gas-gauge and control ICs. Linear Technology's LT1325 contains a gas gauge and charge controller but requires the use of an external µC, typically the keyboard controller.

Note: You'll find essentially three types of individual ICs or chip sets: stand-alone charge ICs, stand-alone gas-gauge ICs, and battery-management ICs. The term *battery management* usually implies that the IC performs both charge control and monitoring of the battery. There are many inexpensive ICs available for charge control, but they don't determine battery capacity.

Some of the products are specialized ICs, and others are µCs specialized for battery-management functions. The MTA11200's design includes the company's 8-bit µC core and, based on a license agreement with Span Inc, uses purely digital methods to integrate battery charge and discharge current. Zilog Inc discusses a smart charger based solely on it Z8 µC in **Ref 2**.

THE DEBATE OVER SMART-BATTERY STANDARDS

Any move toward standardization has its detractors, particularly those who don't want to disclose or change the use of their leading-edge technology. Critics of a standard smart battery object because they want to use a unique power-management scheme. From a manufacturer's point of view, standard battery data-communication protocols and form factors diminish the value that they can add to their products even further.

However, the Duracell/Intel Smart-Battery Specification appears open enough that these critics may not have to worry. The overall standards push has many layers from which OEM developers can pick and choose. In a broad sense, these layers are Intel's System-Management Bus, the battery data set and data-communication protocol, and the physical form factor. You can easily create products that use the SMBus, but don't necessarily conform to the data set in the Intel/Duracell specification or any standard-battery form factor. However, ultimately end users may have the say by demanding that battery packs be reusable in different systems.

Mix-and-match trade-offs

The bq2040 and bq2014 ($4.85 (10,000)) from Benchmarq Microelectronics highlight the trade-offs of various mix-and-match approaches. The 2040 is a gas-gauge IC that meets the Duracell/Intel SMBus interface and Smart-Battery Data specification. The 2014 is a proprietary stand-alone gas-gauge IC. Benchmarq teamed with SystemSoft to develop keyboard-controller software that translates the 2014's data to fit the Duracell/Intel spec. In this approach, the keyboard controller, rather than any IC in the battery pack, performs all the gas-gauge calculations. The bq2014 provides a more minimal data set than the bq2040 and has the minimum features necessary to do effective battery monitoring. Thus, the bq2014 is cheaper and more flexible, but doesn't provide as much information as the bq2040. Another difference that affects system implementation is that the bq2040 can't stop the charge but communicates its full status across the serial bus. The bq2014 can stop its own charging.

Narrowing your choices

When choosing a battery-management approach, you should consider numerous factors, including gas-gauge accuracy; charge control; cost; other required external hardware, such as temperature sensors and stable oscillators; level of standardization or, conversely, flexibility and programmability; development support; and the power consumption of the monitoring circuitry. Other than for development systems, none of the products surveyed with set pricing were over

LOOKING AHEAD

Many design choices exist for implementing smart-battery technology, and these choices will expand this year. Many companies have explicit plans to introduce smart batteries or ICs, many by the end of this quarter (if not already announced). Some notable examples are a charge-control, gas-gauge and protection IC for Li-ion batteries and a charge-control IC for rechargeable alkaline batteries from Benchmarq Microelectronics; May production quantities of smart batteries from Duracell; silicon and battery packs in place for working with OEM developers from Energizer Power Systems; a development system for and production silicon of a two-chip set and a battery-management IC tailored to cellular phones from National Semiconductor; a variety of power-management ICs for the SMBus from Maxim Integrated Products; the MTA14000 battery-management IC compatible with the SMBus and more integrated than the MTA11200 from Microchip Technology; and the TEA1102 desk-top charger IC for all chemistries including Li-ion and lead-acid batteries and the SAA1501 intelligent battery IC from Philips Semiconductors.

One interesting note about smart batteries and recycling: Duracell has announced a take-back program and claims that smart batteries aid in the recycling process by communicating information, such as number of charge/discharge cycles, chemistry, and manufacturer.

SMART-BATTERY TECHNOLOGY

$10 in 10,000-piece quantities.

The monitoring circuit's power consumption can be a big consideration, and you should determine how much operating and shutdown current any battery-management scheme requires. Most of the available ICs have shutdown and shelf-shutdown modes. In a part due this year, Microchip Technology will add a third "hibernate" power mode that draws 5 μA or less.

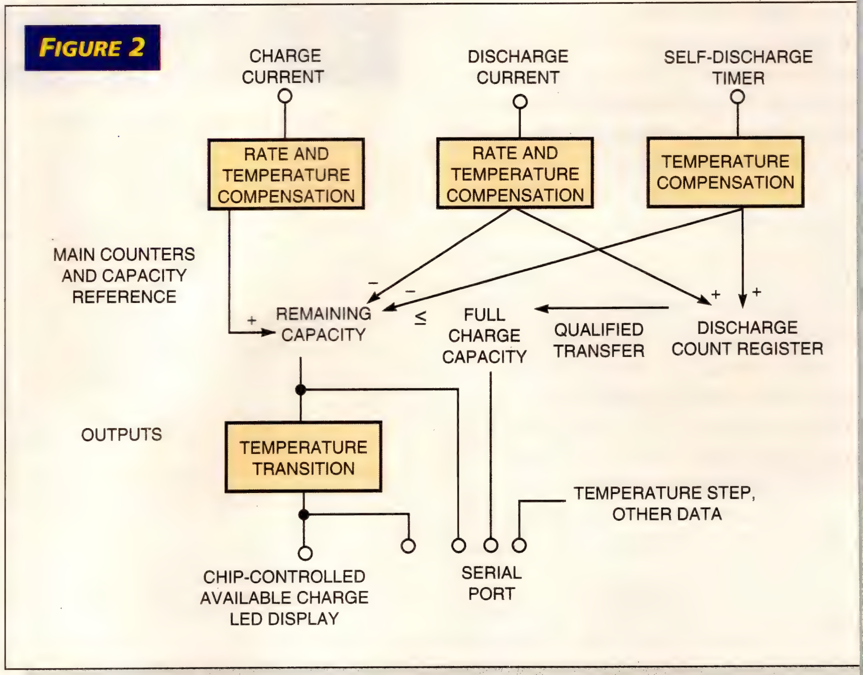
Gas-gauge accuracy is a must

However, the most critical of the considerations are the accuracy of the monitoring circuit and implementation of the charge-control scheme.

For effective battery management, the self-monitoring of the battery—the gas-gauge function—must be highly accurate. Without accuracy, no level of control can improve the battery's performance. To achieve a high level of accuracy, the gas-gauge electronics may have to compensate for changing battery parameters and perform calibration.

A gas gauge measures some battery parameter that it uses to determine and report battery capacity (**Ref 3**). Some older, very inexpensive gas gauges simply measured voltage. This battery voltage is a highly inaccurate indication of a battery's capacity because it changes with temperature and battery load. Most of the more advanced gas-gauging products, including those discussed here, measure the current into and out of a battery to determine its capacity.

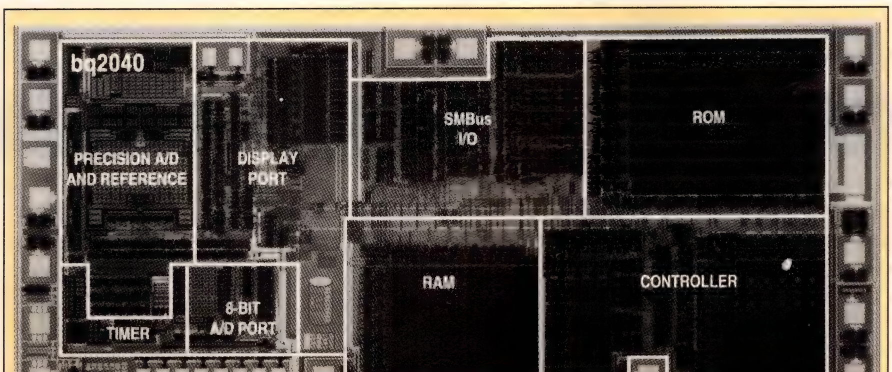
FIGURE 2



This operational overview shows how the bq2040 gas-gauge IC accumulates a me sure of charge and discharge current, and estimates self-discharge while applyi various types of compensation. The IC updates the main counter and registers a outputs the information to an LED or through a serial port.

Some manufacturers call this function *coulomb counting*.

Although measuring current is much more accurate, each manufacturer's implementation and accuracy claims differ. Because of the integration of the battery packs with the control electronics, Duracell claims its smart batteries have extremely high accuracy of around 1%, stemming from their accurate cell models and calculation algorithms. Benchmarq points to the pre sion ADC and reference in the bq20 as the main accuracy-determini components. A V/F converter that us residuals from one conversion for t next conversion actually performs th ADC function. The net result is ze quantization error. Microchip MTA11200 gets within 3% accuracy better by using good internal comp nents and a calibration with extern components. According to Nation Semiconductor, having the data-acq sition portion of the battery-manag ment system residing in the batte pack results in much higher accura than solutions that put this function a separate charger.



The heart of the Benchmarq Microelectronics' bq2040, a gas-gauge and charge-control IC with SMBus interface, is the accurate precision ADC and reference block that performs the gas gauging. This ADC is actually a V/F converter that uses conversion residuals for a net quantization error of zero.

Note compensation

Part of a gauge's accuracy stems fro applying compensation for varyi conditions and calibration. For exam ple, Microchip's MTA11200 adjusts t charge-efficiency calculation based the present state of charge and the te perature. To improve accuracy, the does not apply the compensation fa tors to the state-of-charge calculati when the battery is discharging.

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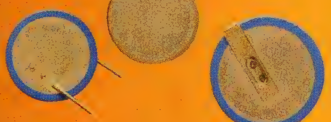

TWICELL

Also, a battery's capacity can vary over its lifetime, and, from time to time, many of these ICs need to self-calibrate and relearn 100% capacity. Benchmarq's bq2040 has an extra register that looks at discharge characteristics (**Fig 2**). If there have been no partial charges of the battery, the IC automatically updates capacity on a full-discharge cycle. When the battery reaches full charge, the IC resets capacity to full.

Capacity measurements *should* err on the conservative side and, after some number of partial charges, the system *should* inform the user that a full discharge is necessary.

Choose the right charge control

Charge-control schemes are also critical. All of the commonly accepted methods measure voltage, temperature, or their derivatives. For example, combinations of the dT/dt (change of temperature with time) and peak-voltage detect or dV/dt schemes (change of voltage with time) are recommended often for many batteries. For a time, negative delta-V, which detects the beginning of a negative voltage slope, was popular. According to some in the industry, the use of this technique appears to be waning in order to prevent overcharge of any battery type, including NiCds.

In addition to effectiveness of the charge control, you may want to choose a management scheme that allows you to change the charge-control regime easily. One of the advantages of National Semiconductor's approach is its flexibility: You can implement many charge techniques. To change the charge-termination scheme, you simply change the EEPROM look-up tables in the 6980. Microchip's MTA11200 allows you to choose charge-control regimes for three battery chemistries and numerical value to stop charging. Changing a small portion of the controlling µC's code changes the LTC1325 charge-control regime.

One final, important point about the charge-control scheme: It must be *the* one recommended by the battery manufacturer. Opinions and battery designs differ in the industry, and one NiMH manufacturer may recommend something slightly different than another. Don't second-guess battery manufacturers.

Another feature of a smart-battery or system is its ability to store and maintain information, such as the number of charge/discharge cycles and temperature exposure extremes. Microchip coins the MTA11200's data-logging function as the "flight recorder" of the battery. This feature, based on external

FOR FREE INFORMATION...

For free information on the battery-management products discussed in this article, circle the appropriate numbers on the postage-paid Information Retrieval Service card or use *EDN*'s Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in *EDN*.

Benchmarq Microelectronics Inc
Carrollton, TX
(214) 407-0011
Charge-control, battery-management ICs
Circle No. 354

Duracell International Inc
Bethel, CT
(800) 431-2656
Smart batteries
Circle No. 355

Energizer Power Systems
Gainesville, FL
(904) 462-3911
Smart Batteries
Circle No. 356

Hitachi America Ltd
Brisbane, CA
(800) 285-1601
Power-management µCs
Circle No. 357

Integrated Circuit Systems Inc
Valley Forge, PA
(610) 630-5300
Charge-control ICs
Circle No. 358

Intel Architecture Labs
Hillsboro, OR
(503) 797-4216
System-Management Bus, Smart-Battery Specs
Circle No. 359

Linear Technology Corp
Milpitas, CA
(408) 432-1900
Battery-management
and charge-control ICs
Circle No. 360

Maxim Integrated Products
Sunnyvale, CA
(408) 737-7600
Charge-control ICs,
SMBus-control ICs
Circle No. 361

Microchip Technology Inc
Chandler, AZ
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Battery-management ICs
Circle No. 362

National Semiconductor Corp
Santa Clara, CA
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Battery-management ICs
Circle No. 363

Philips Semiconductors
Sunnyvale, CA
(408) 991-2320
Charge-control and monitor ICs
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Rayovac Corp
Madison, WI
(608) 275-4693
Reusable alkaline batteries
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Sanyo Energy USA Corp
San Diego, CA
(619) 661-6620, ext 685
Rechargeable battery packs,
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SystemSoft Corp
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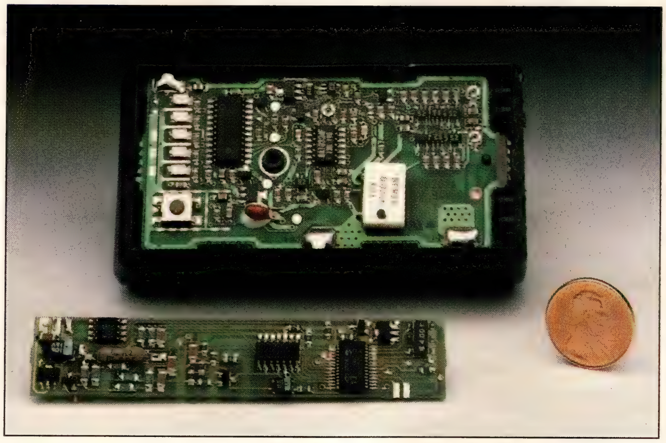
SMART-BATTERY TECHNOLOGY

EEPROM, lets you log a number of charge cycles and check if the battery has gone above or below certain limits.

The EEPROM data tables in National's LMC6980 holds values for load, data, and self-discharge correction. The EEPROM also stores three sets of phase termination and charge rates, min/max voltage and temperature limits, min/max exposure temperatures, and the number of charge/discharge cycles.



High integration and shrinking component size let battery-management functions easily fit in a battery pack. A standard application circuit using Microchip Technology's MTA11200 (bottom) requires much less space than that of a standard camcorder battery pack (top).

Development systems

Development support is available for many of these battery-management schemes, including National's chip set, and Microchip Technology's MTA11200 ($499). Most include Windows-based software and some sort of demo board that includes the control and gas-gauge functions. These systems let you change various control parameters and test how the battery pack performs using those parameters. Benchmarq offers two versions of a development kit for its bq2040: a module ($25 each) that can fit on a pc board, or a larger pc board (the $149 EV2040) that you can hook to a battery pack.

Smart batteries have limits

Keep in mind what "smart" batteries can and can't do. They *can* report accurate state-of-charge information. They *can* implement a charge-control regime.

However, a smart battery or battery-management system *can't* make up for improper design. None of these products is completely fail-safe. For example, when using dT/dt methods to determine the end of charge, you can inadvertently fool the "smart" charger by changing charge rates. Abruptly slowing the charge rate for an almost-full battery may not trip the dT/dt mechanism properly, which results in overcharging. Also, power-supply noise can cause false terminations in peak-voltage-detect chargers.

System design considerations include first determining the appropriate level of battery management. Once you narrow down the choice, you need to determine the impact of various support components. For example, measuring battery current to gauge capacity requires a sense resistor. You have to look at the system's power requirements to choose the right value of this resistor. You want it small enough to not waste power but large enough to produce a decent signal that the system can measure. EDN

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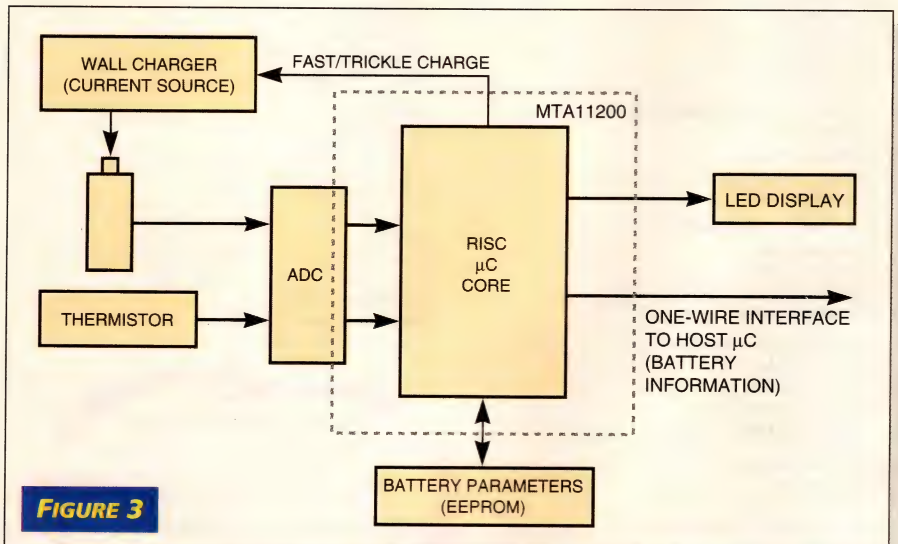

FIGURE 3

Microchip Technology's MTA11200 battery-management IC implements a timed-voltage-ramp ADC that uses an external quad comparator in front of a RISC µC core. External EEPROM stores control parameters that customize the IC for a particular battery type and application.

You can reach Technical Editor Anne Watson Swager at (610) 645-0544.

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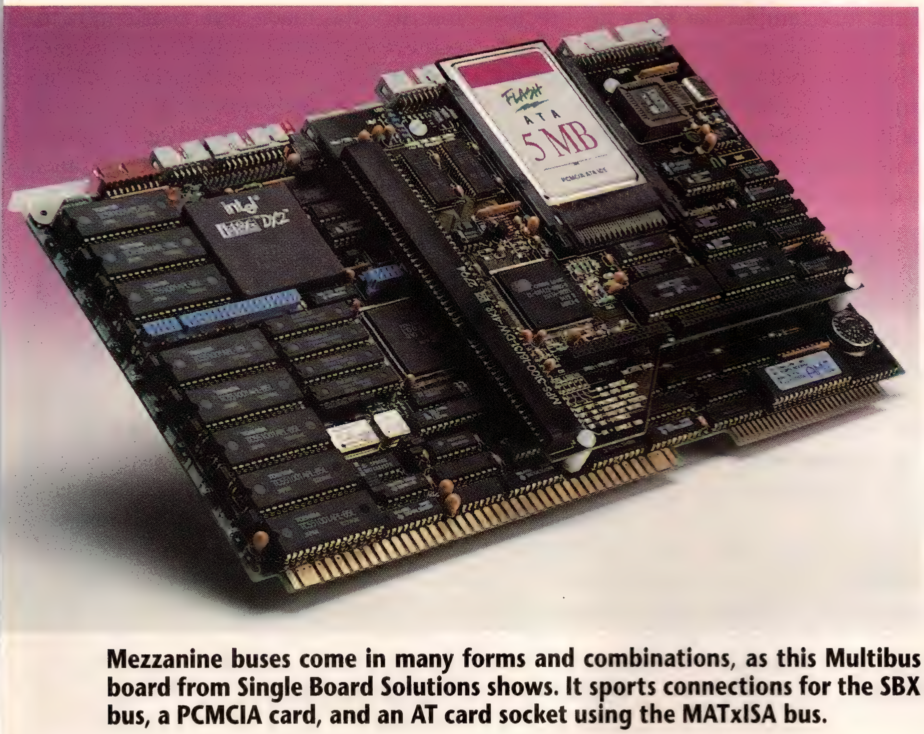
CIRCLE NO. 9

Mezzanine buses bring backplane benefits to the board level

RICHARD A QUINNELL, TECHNICAL EDITOR

Mezzanine buses promise design flexibility and other compelling advantages for backplane-bus board designs. A profusion of competing alternatives, however, has diluted the buses' value.

Like the backplane-bus architectures they mimic, mezzanine buses promise substantial benefits. Backplane buses have already made good on their promise, allowing you to create a customized system by selecting from an array of off-the-shelf boards and plugging them together. The breadth and diversity of the board array provide design flexibility and allow the selective upgrading of hardware functions. Competition between board vendors promotes innovation and lower prices. To achieve these same benefits at the board level, manufacturers have widely adopted the use of a daughterboard on a standard mezzanine bus.



Mezzanine buses come in many forms and combinations, as this Multibus board from Single Board Solutions shows. It sports connections for the SBX bus, a PCMCIA card, and an AT card socket using the MATxISA bus.

The term "mezzanine" comes from the daughterboard's position within the rack. The daughterboard, or mezzanine card, occupies a position between two main cards within the cage, just as a mezzanine in a hotel lies between two main floors. The functions that the mezzanine card can provide depend on the nature of its standard bus. Some mezzanine buses provide an opportunity to add specialized I/O functions. Others

MEZZANINE BUSES

allow upgrading of the main board's CPU and memory.

The mezzanine-bus approach lets you use off-the-shelf modules to customize a base board quickly with the type and amount of I/O or processing you desire. By allowing the mix and match to occur on a single card rather than on several cards in a rack, mezzanine buses increase the space efficiency of off-the-shelf systems. Mezzanine buses further simplify the task of designing a function when off-the-shelf boards don't meet your system needs. Mezzanine-bus cards are smaller, cheaper, and easier to design than are full-size backplane-bus cards.

Mezzanine buses also provide a private data highway for time-critical information that would otherwise be shuttled across the system backplane for processing. The information's movement would suffer delays due to protocol overhead and the need to share the backplane's bandwidth with other system functions. A mezzanine bus can be free of those restrictions.

Overcoming a checkered past

For all of its advantages, however, the mezzanine bus developed an unsavory reputation. Early daughterboards for use on the buses suffered reliability problems due in part to connector failures. The daughterboards also experienced heat buildup in the space between them and the main boards.

Although the stigma of those early years remains, manufacturers have long since solved the problems themselves. The result has been that most board manufacturers have been adopting mezzanine buses since the late 1980s. Even that most demanding of customers, the US military, has accepted the mezzanine concept by qualifying Radstone Technology's MxBus. Indeed, the number of mezzanine buses almost exceeds the number of board vendors. **Table 1** provides a representative sample of available mezzanine-bus structures.

However, the mezzanine-bus approach does have its drawbacks. The ease of hardware customization a mezzanine bus provides comes at the expense of software complications. While a daughterboard may function electrically in any base board with the appropriate mezzanine bus, the software to run the card is not so portable. Mezzanine boards with similar functions from different manufacturers do not typically have the same address and register assignments. Each must, therefore, come with unique drivers. The drivers, in turn, vary with the operating system you use.

That software also varies with the base-board type you use. The software disk that Pentek provides for its products, for example, has separate directories for each of its base boards. Each directory contains sample initialization and data-transfer programs in C for all of Pentek's mezzanine boards with that base board. The result is a matrix of software and drivers covering all the base-board/mezzanine-board combinations.

Exploding software needs

Factoring together the number of base boards, mezzanine boards, mezzanine buses, and operating systems available results in a combinatorial explosion of software requirements. Mezzanine-board vendors cannot provide enough support to allow their customers complete freedom in mixing and matching mezzanine and base boards from different manufacturers. To achieve that degree of flexibility, you're going to have to do some software development. The amount of software development you need to do depends on the level of software support your suppliers provide and on the operating system you use. Suppliers vary in both the amount of software they provide and the range of operating systems they handle. Choosing a popular operating system maximizes your chances of receiving useful off-the-shelf software with your mezzanine boards.

One way to reduce the software complexity of the mezzanine-bus approach would be to standardize the mezzanine bus itself, eliminating one variable. The industry has made several attempts to achieve such a standard. One of the earliest attempts was the Special Application Module (SAM) bus for VME boards in the mid-'80s. The bus was effectively an extension of the 68xxx CPU bus

(continued on pg 72)

LOOKING AHEAD

The introduction of the Peripheral Component Interconnect (PCI) mezzanine-card (PMC) standard generated considerable interest in the embedded-computing community, along with support from major companies and industry organizations. That support alone, however, won't make the standard work. The key to PMC's survival in the market, as with all other mezzanine-bus standards, is market acceptance.

PMC certainly looks promising. Riding on the coattails of the PC industry can make for inexpensive hardware and software in the backplane-bus, embedded-system market. Yet, the PC industry is, for the most part, indifferent to the embedded-system market. Most PC market players take a high-volume, low-overhead, rapid-turnaround stance. As such, they can't afford low-volume, support-demanding, embedded-system customers. Consequently, the PC industry will make its decisions without regard to the embedded-system market's needs. Riding on the coattails may well turn out to be having a tiger by the tail.

PMC can work, but only if the customers want to adopt the PC architecture. Otherwise, the use of the PCI bus structure is more an impediment than an advantage. Many real-time applications cannot use the PC architecture. Consequently, PMC will not replace, but only supplement, the other mezzanine-bus standards. Its ultimate success will depend on the success of the PC architecture in the embedded-system market and on a reliable supply of components.

TABLE 1—REPRESENTATIVE MEZZANINE BUSES

Name	Base-board type	Address lines	Data lines	Multi-plexer	Inter-rupts	DMA channels	Bus speed (Mbytes/sec) (Note 1)	Address space (bytes)
Apex	VME	32	32	N	1	-	20	4M
CMI bus	PC	32	16	N	9	6	1.544	1024
Corebus	VME	32	64	N	4	-	132	4G
CXM	VME	24	16	N	-	-	N/S	N/S
Dbus	VME	32	32	N	2	Any	40	N/S
EZ bus	VME	32	32/64	N	2	Any	66/120	500M
HKCM	VME	16	16	Y	-	-	10	N/S
HSI	VME	32	32	N	3	-	100	16M
Industry Pack	VME	24	32	N	4	4	64	16M
IPIN	VME	32	32	N	1	-	20	16M
M-Modules	Multibus/ VME	24	32	Y	1	1	80	16M
MATxISA	Multibus	24	8/16	N	11	7	4	16M
MAXPack	VME	32	32	N	2	-	128	64M
MIX	Multibus/ VME	32	32	N	6	6	12	256M
MODULbus	VME	8/16	16	N	1	1	8	512
MxBus	VME	32	32	N	1	1	31	64M
PC/104	(Note 4)	20	8	N	6	3	N/S	N/S
PMC	Multibus/ VME	32/64	32/64	Y	4	-	132/264	4G
SBX	Multibus	3	8/16	N	2	1	8	16M
SCIM	VME/STEbus	24	16	N	3	1	10	256M
Squall II	VME	32	32	N	2	0	66	256M

Notes:
1. Bus data rate is for sustained transfers.
2. I/O space not listed if memory mapped.
3. Size is for standard single-width module; larger sizes may be available.
4. Designed as a stackable, stand-alone module set; PC/104 modules are also being used as mezzanine cards in larger systems.
N/S=not specified

I/O space (bytes) (Note 2)	Voltages	Pins	Module size (Note 3)	Stack height	Open standard	Standard-control organization	Other
-	5, ±12	100	104×97 mm	-	Y	Radstone Technology	
-	±12	62	1.55×4 in.	-	Y	Computer Modules	
-	5, ±12	250	3.7×6.1 in.	-	Y	Heurikon	Front-panel I/O access
-	5	96	100×100 mm	7	Y	VITA	68302/ 68360 local bus
-	5, ±12	96	3U/6U	-	Y	Matrix	Front-panel or P2 I/O
4M	5, ±12	256	3.5×5.6 in.	2	Y	Synergy Microsystems	16/32-byte burst to 133 Mbytes/sec
N/S	5	256	3.7×6.1 in.	-	Y	Heurikon	Accepts PCM-CIA cards
-	5, ±12	240	6.3×8.22 in.	-	N	Vista Controls	AM29000 processor interface
64k	5, ±12	50	1.8×3.9 in.	-	Y	VITA	
-	5, ±12	100	53.34×148.35 mm	-	N	Eltec Elektronik	
256k	5, 12	60	144.5×42.9 mm	-	Y	MUMM	Intermodule port, trigger I/O
64k	±5, ±12	62	6.4×7.1 in.	-	N	Single Board Solutions	Accepts standard ISA board
-	5, 3.3, ±12	200	5.8×3.9 in.	-	N	DY4 Systems	Ruggedized, module can be bus master
1k	5, ±12	130	8.9×3.75 in.	3	Y	Intel, MMG	Supports built-in self-test
-	5, ±15	40	110×55 mm	-	Y	MODULbus Association	ESD-shielded
-	±5, ±12	224	122×89 mm	-	Y	Radstone Technology	Convection-cooled option; MIL-qualified
N/S	5, ±12	64	3.6×3.8 in.	3 to 5	Y	PC/104 Consortium/ IEEE P996.1	PC compatibility
N/S	5 or 3.3, ±12	128/256	75×150 mm	-	Y	VITA, MMG, IEEE P1386.1	Based on PCI bus; allows front-panel I/O
16	5, ±12	50	2.87×3.7 in	-	Y	IEEE 959	
64k	5, ±12	80	120350 mm	-	Y	Arcom	Ruggedized for industrial use
-	5, ±12	100	3.333.85 in	-	Y	Cyclone Microsystems	I/O can seize local bus

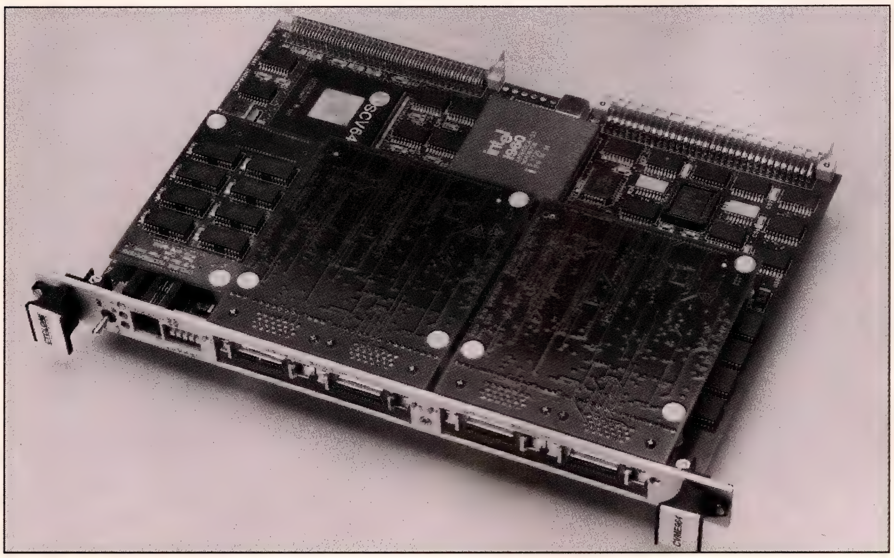
TABLE 2—MEZZANINE-BUS-CARD TYPES

	Module types							
Name	**CPU**	**Memory**	**Digital I/O**	**Analog I/O**	**Network**	**Graphics**	**DSP**	**Other**
Corebus			X	X	X			GPS, SCSI
Industry Pack	X	X	X	X	X	X	X	ARINC, 1553, motion control
M-Modules	X	X	X	X	X	X	X	ARINC, T1, motion control
MIX		X	X	X	X		X	Terminal control,
MODULbus	X	X	X	X	X	X		Motion control
PC/104	X	X	X	X	X	X	X	PCMCIA
PMC		X	X	X	X	X	X	SCSI, motion control
SBX	X	X	X	X	X	X	X	SCSI, motion control

Note: Price range reflects typical commercial-grade boards; prices for ruggedized and military-grade boards can range to $5000.

for VME boards, however, and was limited to boards using that CPU family. It eventually faded from the market.

The late '80s saw the emergence of other mezzanine buses that their creators released as open architectures to create de facto standards. **Table 2** lists several of these buses, along with some of the companies that have adopted the architectures. Two of the most popular architectures, Greenspring's Industry Pack bus and MEN Mikro Elektronik's M-Modules, are approaching true industry standardization. Makers of M-Modules have banded together to form the Manufacturers and Users of M-Modules (MUMM) association, which has taken over the M-Module standard. Both MUMM and Greenspring are now working within the VMEbus International Trade Association (VITA) to develop their specifications for submission to ANSI as international standards.



The function of mezzanine cards varies. This board from Cyclone Microsystems shows two serial I/O ports on Squall bus modules and extended memory on another mezzanine bus.

The IEEE has also made an attempt to standardize a mezzanine card. The IEEE's proposal P1386 attempts to define a common mezzanine card (CMC) that works on VME, Futurebus+, Multibus, and other backplane-bus boards. The base specification describes only the mechanical dimensions and connector requirements, however, and allows two electrical specifications. P1386.2 describes the SBus mezzanine card (SMC), which marries the SBus to CMC. P1386.1 describes the Peripheral Component Interconnect (PCI) mezzanine card (PMC), which uses the PC PCI bus.

The PMC standard saw considerable industry endorsement at its introduction in September 1994. Both VITA and the Multibus Manufacturers Group (MMG) backed PMC. In addition, 13

Price range (Note 1)	Representative vendors
$1000 to $1500	Heurikon, Vista Controls
$350 to $800	Acromag, Ariel, Ballard Technology, General Standards, Greenspring Computers, Motorola, Snijder Micro Systems, Technology 80, Vigilant Technologies
$100 to $3000	AcQuisition Technology, Centralp, Eltec Elektronik, or Industrial Computers, MEN Mikro Elektronik, Philips Industrial Automation
$850 to $2000 T1	Intel, Pentek, Threshold Technology
$70 to $300	Eltec Elektronik, Janz Computer
$100 to $500	Ampro, Comark, WinSystems
$500 to $2000	Aeon Systems, Brand Innovators,Centralp, Compcontrol, Concurrent Technologies, Creative Electronic Systems, Digital Equipment Corp, Force Computers, General Standards, Heurikon, Interphase, Intel, Motorola, or Industrial Computers, Pentek, Radstone Technology
$180 to $500	Intel, Microdesigns, Single Board Solutions, Technology 80, WinSystems, Zendex

manufacturers announced product plans that included PMC, although not all are yet available. A number of other companies have since jumped on the PMC bandwagon.

The goal in transforming the PCI bus to a mezzanine bus is to take advantage of the tremendous economies of scale that the PC industry provides. By adopting PMC, board vendors can readily apply PCs' highly integrated graphics, mass storage, and I/O chips to the embedded market. The PMC bus is electrically identical to the PCI bus, so designers can readily transfer PCI designs to PMC. Further, the diversity of software for PCI-based PC products becomes available for PMC-based embedded products. Despite widespread industry enthusiasm, however, PMC has its share of skeptics who point out a dark side to the rosy picture PMC's proponents paint. Like the benefits, the dark side stems from PMC's attempt to leverage the PC community's innovations.

The first drawback skeptics cite is that the PC industry is highly volatile. In contrast to the 10- to 15-year product life that many embedded-computing customers demand, the PC industry often changes its products several times a year. As the underlying PC components evolve or become extinct, that turnover places in question the long-term availability of PCI parts for PMC cards.

Another drawback of PMC is that PC-component manufacturers typically handle only the DOS and Windows operating systems and have only a slight recognition of Unix. They are virtually indifferent to such popular embedded operating systems as VxWorks, OS-9, and VMEexec. If your system is not PC-compatible, you may face a considerable software-design effort to employ the highly integrated, complex-to-program ICs for PCI.

Skeptics' other concerns about PMC center on the cost and complexity of custom designs. Many embedded-system integrators want to build their own mezzanine boards. PMC skeptics point out that PCI interface chips are still relatively expensive ($50 in quantity). Designing your own interface, they warn, is a complex task. Further, the PCI bus limit of 10-pF input capacitance per pin for an interface card precludes designing a PCI-compliant PLD-based custom interface, because high-speed PLDs typically have a 12-pF input capacitance.

Whether the promises or the concerns over PMC will win out remains to be seen. One thing is already clear, however. Neither PMC nor any other mezzanine bus will achieve the distinction of becoming the sole standard. None of the open standards satisfies everyone's needs. Indeed, manufacturers and standards groups are continually proposing new mezzanine buses, including Ziatech's Ruggedized PCI bus and the MMG's PCI-like MIX-2. At best, several mezzanine buses will coexist.

Further, the board industry is partially resistant to mezzanine-bus standardization, despite the customer benefits standardization entails. Some of the resistance comes from genuine differences in customer requirements. PCI is costly overkill for some customers' needs, for instance, and Industry Pack has limited bandwidth. But other resistance comes from the vendors' attempts to hold onto proprietary designs and compete on the basis of function and performance instead of cost. In either case, widespread adoption of standards is slow, and mezzanine buses have yet to fulfill their promise. EDN

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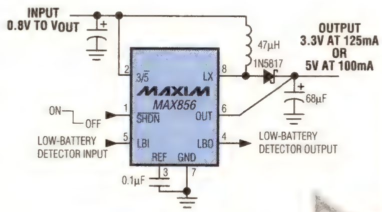
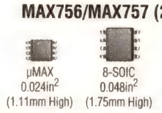
- 1µA Shutdown
- $1.60† (MAX856-MAX859)
- MAX856EVKIT-MM
- See also: MAX856-MAX859 & MAX756/MAX757 (250mA)

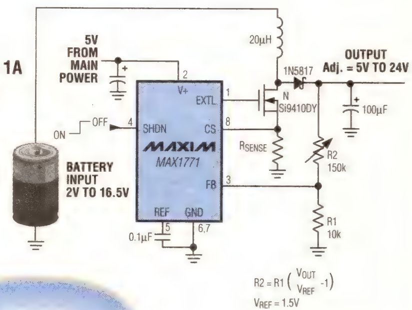




24V Positive LCD Bias Supply

Input: 2V to 16.5V
Output: 5V to Unlimited
Up to 2A

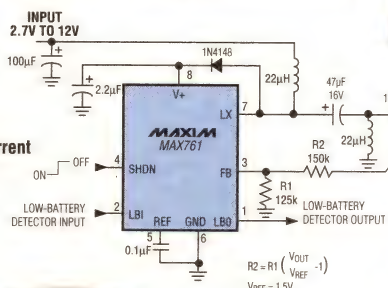
- >90% Efficient from 10mA to 1A
- 110µA (max) Supply Current
- 5µA (max) Shutdown
- Voltage Limited Only by External Power FET V_{GS}
- 300kHz Current-Limited PFM Control
- $1.80†
- See also: MAX1771 & MAX770-MAX773



Step Up/Down 3 Cells or 4 Cells to 3.3V or 5V

Input: 2.7V to 12V
Output: Adj. (1.5V to 6V)
Up to 200mA

- Step-Up/Down Without Transformer
- 85% Typical Efficiency
- 100µA (max) Quiescent Current
- 5µA (max) Shutdown
- No Leakage Through Diode in Shutdown
- $2.09†
- See also: MAX761/762, MAX1771 & MAX877/878/879



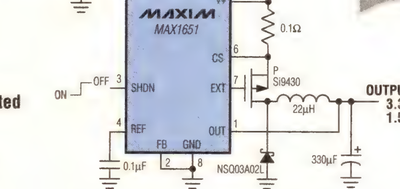
LOW-POWER HAND-HELD DEVICES

- Organizers
- Palmtops
- Medical Meters
- Remote Controls

Step Down 4-Cell to 8-Cell Inputs to 3.3V or 5V

Input: 3.5V to 16.5V
Output: 3.3V, 5V, or adj. (2.7V to V_{IN})
Up to 2A

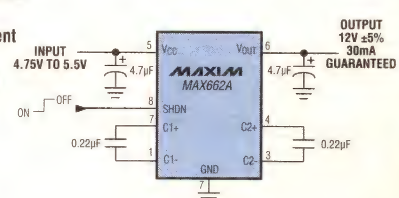
- >90% Efficiency from 10mA to 1.5A
- 100µA (max) Supply Current
- 5µA (max) Logic-Controlled Shutdown
- 8-Pin SOIC
- 300kHz Current-Limited PFM Control
- $1.60†
- MAX1649EVKIT-SO
- See also: MAX1649/MAX1651



5V & 12V Flash Memory Programmers Use No Inductors—Fit in 0.1in2

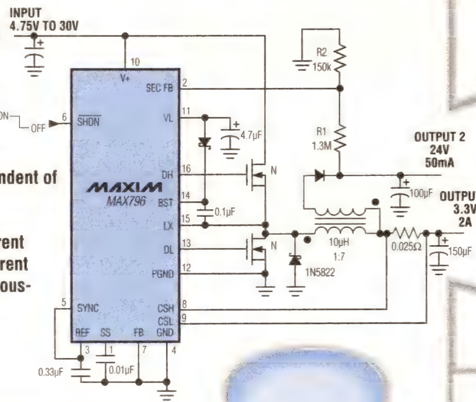
Input: 4.5V to 5.5V (MAX662A)
2V to 3.6V (MAX619)
Output: 12V @ 30mA (MAX662A)
5V @ 50mA (MAX619)

- 185µA (typ) Supply Current (MAX662A)
- 75µA (typ) Supply Current (MAX619)
- 0.5µA Logic-Controlled Shutdown
- $2.09† (MAX662A)
- $1.60† (MAX619)
- MAX662AEVKIT-SO MAX619EVKIT-SO
- See also: MAX619 & MAX662A



Supply 3.3V & 24V from 5-Cell to 30V Inputs

Input: 4.5V to 30V
Output: 3.3V @ 2A (or up to 10A)
24V @ 50mA (adj. 5V & up @ 150mA)

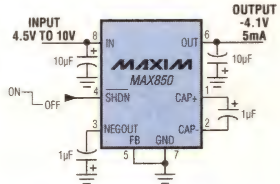


- Optional Dual Output from Single IC
- Secondary Load Independent of Primary Load
- >90% Efficiency
- 300µA (typ) Supply Current
- 3µA (typ) Shutdown Current
- All N-Channel Synchronous-Rectified PWM Control
- 16-Pin Narrow SOIC
- $3.65†
- MAX796EVKIT-SO
- See also: MAX796-MAX799 & MAX767

Complete GaAsFET Bias Supply in One 8-Pin SOIC

Input: 4.5V to 10V
Output: -4.1V @ 5mA or adj. (-1.2V to -9V)

- Fits in 0.1in²
- Replaces 8 Components & 2 ICs
- Low-Noise: 2mVp-p Output Ripple
- 1µA (max) Shutdown Current
- 8-Pin SOIC
- $1.65†
- MAX850EVKIT-SO
- See also: MAX850-MAX853

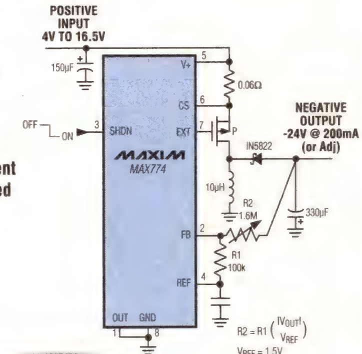


HIGH-POWER WIRELESS COMMUNICATORS

- PDAs
- Cellular Phones
- Subnotebooks
- Personal Digital Communicators

Negative LCD Bias Supply Is 83% Efficient

Input: 3V to 16.5V
Output: 0V to Unlimited Up to 1A

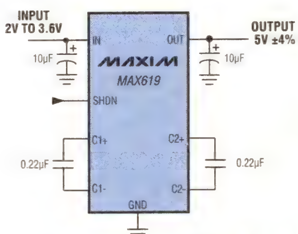


- 83% Efficient from 10mA to 200mA @ -24V
- 100µA (max) Supply Current
- 5µA (max) Logic-Controlled Shutdown
- 8-Pin SOIC
- 300kHz Current-Limited PFM Control Scheme
- $2.20†
- MAX774EVKIT-SO
- See also: MAX774-MAX776

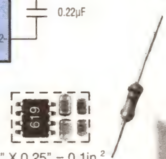
Compact 5V Backup Supply Fits in 0.1in²

Input: 2V to 3.6V
Output: 5V @ 50mA ($V_{IN} \geq 3V$)
5V @ 20mA ($V_{IN} \geq 2V$)

- No Inductors
- 1µA (max) Logic-Controlled Shutdown
- 75µA (typ) Supply Current
- Inexpensive: $1.60†
- MAX619EVKIT-SO
- See also: MAX619



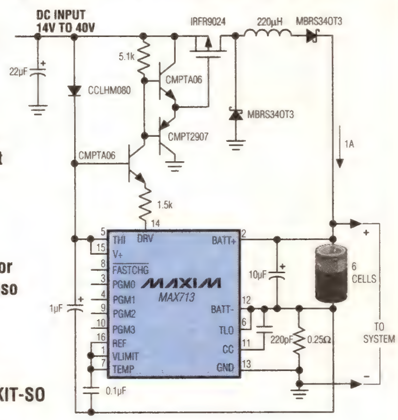
ACTUAL SIZE OF COMPONENTS (RESISTOR SHOWN FOR SCALE)



0.4" X 0.25" = 0.1in²

Complete Charger in 16-Pin Narrow SOIC

Input: 7V to 40V
Output: 1 to 16 Cells Up to 2A



- High-Current (over 1A)
- Temp, Voltage Slope, Timeout Termination
- All Charging Algorithms On-Chip
- Linear Regulator Applications Also Available
- Low-Cost IC & Components: $3.09†
- MAX713SWEVKIT-SO
- See also: MAX712/MAX713

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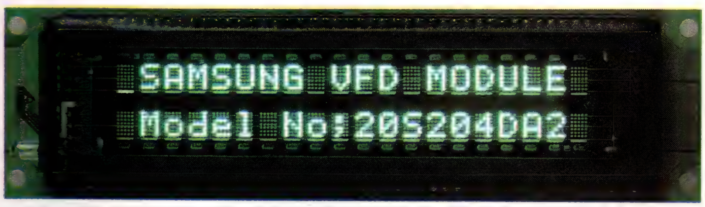

VFD MODULES

MODEL	CHARACTER FORMAT & SYMBOLS	No of Digits (Row X Column)	CHARACTER DIMENSIONS			OUTER DIMENSIONS			ELECTRICAL CHARACTERISTICS			INTERFACE				
			CH (mm)	CW (mm)	CP (mm)	L (mm)	H (mm)	T (mm)	Vcc (Vdc)	Icc (mA)	L (Typ) (ft-L)	Parallel Input	Serial Input	Self Test	Device Select	Busy Out
20S102MA4		1×20	5.0	3.5	4.7	150.0	30.0	26.6	5.0	150	200	○	○	○	○	○
20S204DA2		2×20	5.0	3.5	5.1	155.0	43.0	28.0	5.0	350	250	○	○	○	○	○
40S102MA4		1×40	5.05	3.55	4.75	240.0	40.0	30.0	5.0	350	200	○	○	○	○	○
40S201MA4		2×40	5.05	3.55	4.75	240.0	60.0	29.0	5.0	800	200	○	○	○	○	○
12L101MK1		1×12	11.4	8.7	12.5	200.0	50.0	28.6	5.0	550	250	○	○	○	○	○

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CIRCLE NO. 104

EDITED BY CHARLES H SMALL & ANNE WATSON SWAGER

Notch filter is dc accurate

GARY SELLANI, MAXIM INTEGRATED PRODUCTS, SUNNYVALE, CA

Most active filters exhibit noise, distortion, gain error, and dc offset. However, a filter topology that separates the dc and ac paths can eliminate the last two of these unwanted behaviors (**Fig 1a**). The dc path in this circuit has no op amps and, therefore, no dc offset. The dc path does not have a dc gain error other than –6 dB of attenuation that the R_1/R_2 divider causes. (This attenuation is absent if you omit the R_2 termination.) The ac path consists of C_1 and a synthetic inductor comprising two wideband transconductance amplifiers and associated components. The result is an active circuit that emulates the passive filter of **Fig 1b**.

Simulating the inductance avoids the use of an actual inductor, which can act as a transmitting and receiving antenna for EMI. The equivalent inductance L_{EQ} equals $C_2/(gm_1 \times gm_2$, where gm_1 and gm_2 are the transconductances produced by IC_1 and IC_2. The inductance value can be large if $gm_1 \times gm_2$ is much less than 1, but one end of the network must always connect to ground. Each gm is set by an external resistor (R_3 and R_4 for IC_1 and IC_2, respectively) according to the relationship gm=8/R.

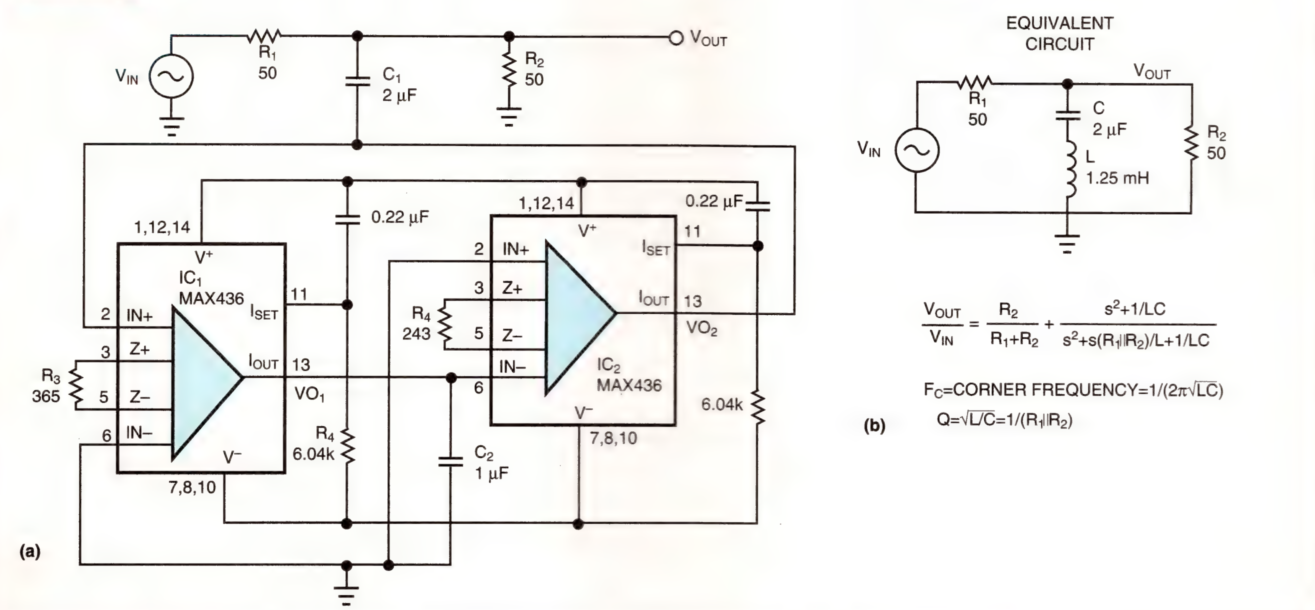
For optimum noise performance, the gm values should allow a full range of output swing for each amplifier. Starting with equal gm values, simulate the filter in Spice using "g" elements for the amplifiers. Observe the peak voltage at each amplifier's output while sweeping the frequency at least one decade above and below the filter's corner frequency (in this case, 3.2 kHz.)

The overall filter determines the peak voltage across the synthesized inductor at pin 13 of IC_2. Therefore, you adjust the peak value at IC_1's pin 13 to match that of IC_2 by varying the gms. Let K equal the ratio of these peak values, which are $VO_1(PK)/VO_2(PK)$. Gain is proportional to transconductance, so divide gm_1 by K and multiply gm_2 by K. Then, rerun Spice with the new gm values to verify that the peaks are equal and the filter shape hasn't changed.

Testing of the entire filter—the source/load connection shunted by the series network of C_1 and the synthetic inductor—on a network analyzer that includes the 50Ω R_1 and R_2 resistors shows a second-order notch response. The rejection at the 3.2-kHz corner frequency is about 40 dB. The parasitic capacitance between the synthetic inductor's output and ground is the main contributor to high-frequency error. This error, though small, increases as the parasitic reactance approaches the parallel combination of the R_1 and R_2 source and load resistances. To minimize error in the frequency response, you should keep these resistances small with respect to the amplifiers' 3-kΩ output impedances. (DI #1665) EDN

To Vote For This Design, Circle No. 405

FIGURE 1



$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2}{R_1+R_2} + \frac{s^2+1/LC}{s^2+s(R_1 \| R_2)/L+1/LC}$$

F_C=CORNER FREQUENCY=$1/(2\pi\sqrt{LC})$

$Q=\sqrt{L/C}=1/(R_1 \| R_2)$

IC_1, IC_2, and related components constitute a synthetic inductor that is part of this dc-accurate notch filter (a). The circuit in (b) is the equivalent passive filter.

DC input controls efficient battery charger

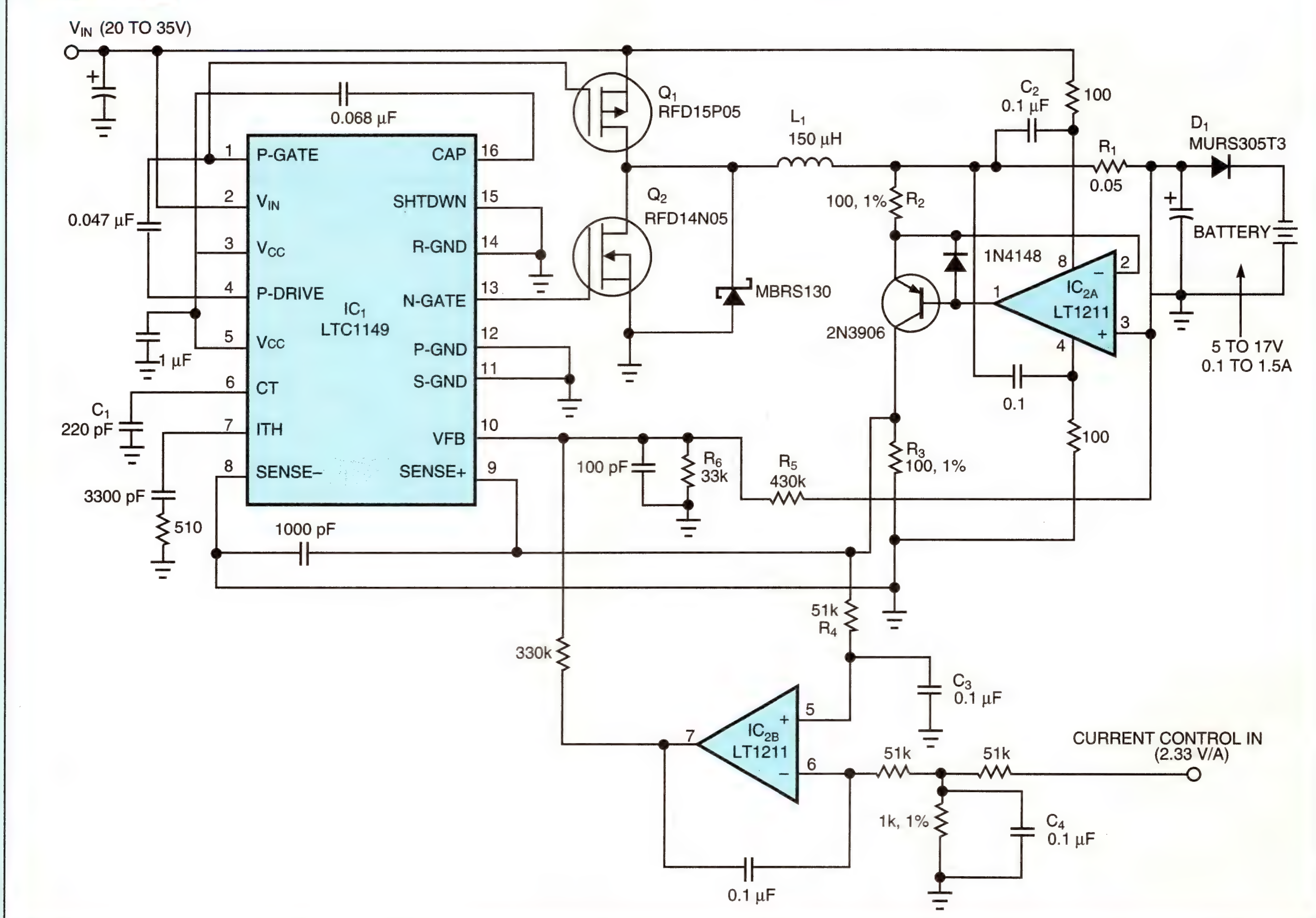
DIMITRY GODER, LINEAR TECHNOLOGY CORP, MILPITAS, CA

Designing a single-rate battery charger by using a current-mode switching-regulator controller is usually not a challenge. If operating at its current limit, the controller provides a constant output current that you can easily adapt to battery charging. However, the design gets more complicated if you must vary the charging current by using a dc control signal. This task is especially difficult with high battery voltages. Providing high-side charging-current sensing to eliminate sense resistors in series with battery ground is desirable.

The circuit in **Fig 1** solves this problem by providing a simple means to control accurately a battery's charging rate. The circuit converts a high-voltage input source to constant current for charging battery stacks of five to 12 cells. The circuit's high efficiency, which varies with the charging current and voltage across the battery, minimizes the power dissipated in surface-mount components. Efficiency measures 92% for a 10V output, the middle of the operating range, and a full 1.5A of load current.

The circuit is based around IC_1, a step-down controller IC featuring fully synchronous rectification, current-mode control, and a constant off-time architecture. During IC_1's on time, Q_1 conducts, and current builds in L_1. When this current reaches the value preset by IC_1's on-chip error amplifier, Q_1 turns off and the current flows through Q_2. C_1 determines the off time, which is fixed. L_1 integrates current pulses from Q_1 to provide essentially constant output current. D_1 pre-

FIGURE 1



This circuit, based around the operation of a step-down switching-regulator controller, provides a simple, accurate control of a battery's charging rate.

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- *Best* Input Capacitance (<2pF)
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		CONV. RATE (Msps)	INTERNAL T/H	50Ω INPUT	EFFECTIVE BITS	SINAD (dB @ F_{IN})	INPUT BW (MHz)	JITTER (ps)	INPUT CAP (pF)
Maxim	**MAX101**	**500**	**Yes**	**Yes**	**7.1**	**44.5 @ 250MHz**	**1200**	**< 2**	**< 2**
Maxim	**MAX100**	**250**	**Yes**	**Yes**	**7.1**	**44.5 @ 50MHz**	**1200**	**< 2**	**< 2**
Harris	HI1276	500	No	No	5.8	37 @ 100MHz	300	11	20
Sony	CXA1276K	500	No	No	6.4	40 @ 100MHz	500	5	16
SPT	SPT7750	500	No	No	6.3	40 @ 250MHz	900	2	15

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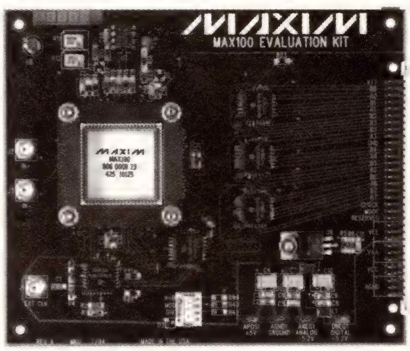

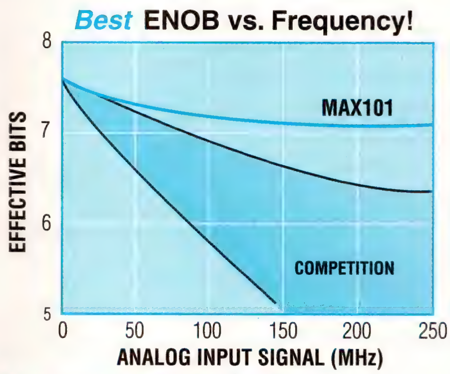

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CIRCLE NO. 94

vents the batteries from discharging through the feedback divider network when the charger is shut down or the input power is removed.

IC_1's sense pins usually sense the current in L_1 as a voltage across current-sense resistor R_1. However, the current-sensing pins have a common-mode range limited to 13V. To accommodate higher output voltages, **Fig 1** uses a special current-sensing circuit. A precision high-frequency amplifier, IC_{2A}, forces the voltage across R_2 to equal that across R_1. Neglecting Q_1's base current, the same voltage appears across the now ground-referenced R_3. The common-mode range of the amplifier is not exceeded because the input powers IC_1. To improve high-frequency noise immunity, C_2 and C_4 filter out any high-frequency common-mode signals.

IC_{2B} senses the average output current using the R_4/C_3 lowpass network and servos this current versus the control input. When you remove the battery, IC_{2B}'s output goes to ground, and the feedback resistors R_5 and R_6 clamp the output at a fixed level. If you omit these resistors, the output rises close to the input when the battery is disconnected. This circuit preserves output-current regulation with battery voltages within 1V of the input voltage. (DI #1662) EDN

To Vote For This Design, Circle No. 406

Bit reverser scrambles data for FFT

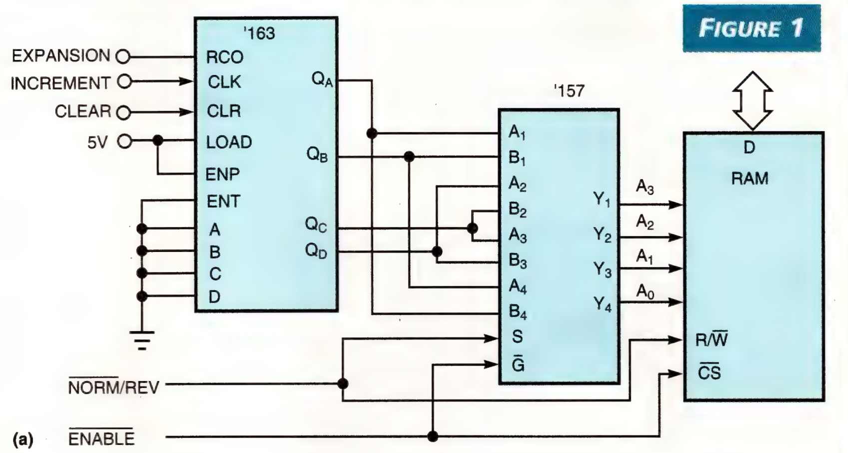
Alan Land, CRS Electronics, Pittsburgh, PA

The hardware bit-reverse and linear-address generator in **Fig 1a** scrambles a time-domain digital N-sample record. The circuit is primarily meant to scramble data before taking a real-time butterfly FFT and can follow a formerly published *EDN* Design Idea ("DAC and µP implement hardware window generator," March 31, 1994, pg 58).

Fig 1a shows only one stage of the possible address range. For records greater than 16, you can simply cascade more counters and add more multiplexers. The trick is to produce the mirror image of the normal binary up count, as **Fig 1b** shows. A simple wiring trick replaces a time-consuming program that requires many memory moves. **Fig 1c** shows how to expand the wiring to addresses greater than 16. The circuit reads the time-domain record into the RAM using linear addresses when NORM/REV is low. The circuit reads the data out using bit-reverse addresses when NORM/REV is high. Pulsing the '163's clock increments each address. You can descramble the record by writing the RAM using the linear address then reading it back using bit reverse. (DI #1663) EDN

To Vote For This Design, Circle No. 407

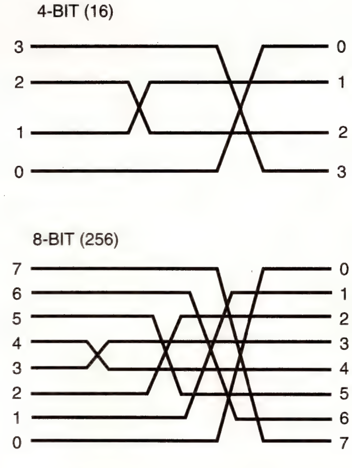
FIGURE 1



(a)

NORM	REV
0000	0000
0001	1000
0010	0100
0011	1100
0100	0010
0101	1010
0110	0110
0111	1110
1000	0001
1001	1001
1010	0101
1011	1101
1100	0011
1101	1011
1110	0111
1111	1111

(b)



(c)

The simple circuit in (a) scrambles records prior to taking an FFT, using a trick that produces the mirror image of a normal binary up count (b). You can use the connections in (c) to expand the wiring to addresses greater than 16.

Spice models power MOSFETs

RICHARD K WILLIAMS, IRAJ MASARRATI, AND AJAY BUTANI, SILICONIX INC, SANTA CLARA, CA

BBS

The Spice macromodel in **Fig 1** accurately simulates double-diffused (DMOS) power-MOSFET transistors. Although you can easily get Spice models for just about any op amp, power-MOSFET Spice models are virtually nonexistent.

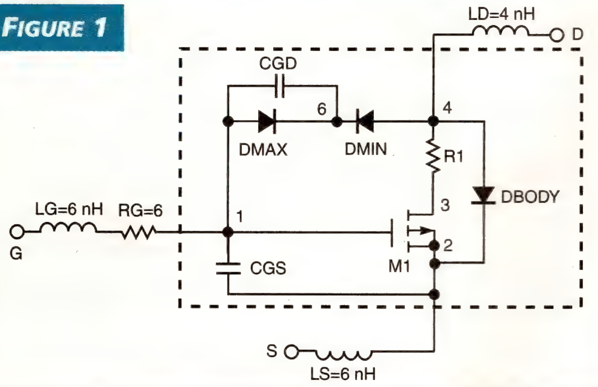
The basis for the model is the principle that the lower-valued of two voltage-variable capacitors in series dominates the string's net capacitance. Two back-to-back diodes, DMIN and DMAX, achieve this variable-capacitance effect. Aside from some negligibly small leakage currents, the diodes never conduct dc through their series network. Regardless of the polarity of applied voltage, one diode always remains reverse-biased.

Because no substantial steady-state current flows, you can envision the DMIN/DMAX network as a capacitive voltage divider. Whenever the MOSFET's drain voltage is high, diode DMIN is reversed-biased, giving it a low capacitance. If the node between the two diodes tries to float positive, diode DMAX becomes forward-biased and holds the node near ground. The low capacitance of DMIN then overpowers the higher capacitance of DMAX, resulting in the desired low equivalent capacitance.

In essence, the DMIN capacitor describes a MOSFET's highly voltage-variable capacitance in the off or saturated region of operation. Meanwhile, the DMAX diode's capacitance models the maximum capacitance value in the linear region of operation.

The DMIN model is semiphysical because it emulates the behavior of the drain-to-body depletion spreading within the MOSFET. For operating conditions where the MOSFET's gate voltage exceeds its drain voltage, the sign of V_{GD} reverses and DMIN becomes forward-biased, increasing its capacitance. Because DMAX becomes reverse-biased, its capacitance decreases to a value lower than DMIN's.

FIGURE 1



This Spice macromodel simulates power MOSFETs. Two back-to-back diodes, DMIN and DMAX, achieve a variable-capacitance effect that models the device's complex gate capacitance.

By choosing the value of DMAX to be relatively voltage-independent, the overall capacitance of the network approaches a constant value, CMAX, which the capacitance of the DMAX diode determines. This constant maximum capacitance is consistent with the formation of the drain-accumulation layer under the gate of a vertical DMOS device operating in its linear region.

The additional capacitance in parallel with the DMAX diode provides some further curve-fitting capability. Because the node between the diodes is never completely floating,

LISTING 1

```
.SUBCKT SI9400P 4 1 2
M1 3 1 2 2 PMOS W=283000U L=1U
R1 4 3 RTEMP .018
CGD  1 6 800PF
CGS  1 2 70PF
DMIN 4 6 DMIN
DMAX 1 6 DMAX
DBODY 4 2 DBODY
**************************************************************
.MODEL pmos        pmos    (level=  3          TOX     = 5E-8
+ RS      = 0.023          RD      = 0.0       LD      = .7E-7
+ WD      = 0              NSUB    = 1E16      VTO     = -3.1
+ UO      = 240            VMAX    = .7E7      delta   = .1
+ XJ      = 1.3E-6         KAPPA   = 1.000     ETA     = 0.014
+ THETA   = .47            TPG     = -1        NFS     = 6E10
+ CGSO    = 0.0            CGDO    = 0.0       CGBO    = 0.0
+ GAMMA   = 1              PHI     = .5        IS=0 )
**************************************************************
.MODEL DMIN D (CJO=800E-12     VJ=0.50     M=0.75
+  FC=0.5  IS=1E-21  )
**************************************************************
.MODEL DMAX D (CJO=10E-12     VJ=0.50     M=0.50
+  FC=0.5          IS=1E-14          TT=10E-9          )
**************************************************************
.MODEL DBODY D (CJO=1100E-12      VJ=0.504     M=0.487
+  FC=0.5      IS=1E-8      N=1.5         TT=19E-8       BV=28 )
**************************************************************
.MODEL RTEMP RES (TC1=6E-3          TC2=3E-5)
**************************************************************
.ENDS
```

FIGURE 2

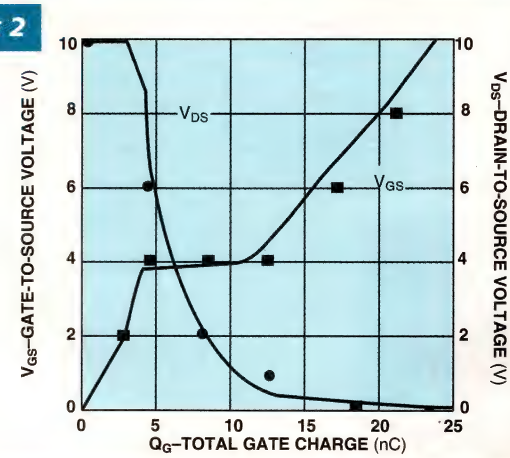


Fig 1's model is accurate for transient operation in switching applications. This graph compares a measured DMOS' gate-charge curve (dots) to the macromodel's output (solid lines). Notice the good agreement, even in the plateau region of the gate-charge curve where the drain voltage is rapidly changing.

you do not need to initialize it to run a simulation. You must adjust the capacitance parameters to fit observed data when modeling a given MOSFET.

Because switching applications predominate for power MOSFETs, the model must be accurate for transient operation. **Fig 2** compares a measured DMOS's gate-charge curve (dots) to the output of its corresponding power-MOSFET macromodel's (solid lines). Notice the good agreement even in the plateau region of the gate-charge curve where the drain voltage is rapidly changing.

Fitting this region is extremely important because the influence of CGD can triple the effective input capacitance of the device. In a high-speed switch-mode power supply, for example, failure to account for CGD can lead you to grossly underestimate power losses associated with driving the power MOSFET's gate.

The compressed ZIPfile attached to **EDN BBS /DI_SIG #1656** contains a detailed write-up and **figures** along with HSpice and PSpice listings for specific devices. **Listing 1** is an example Spice model for an SI9400P. (DI #1656) EDN

To Vote For This Design, Circle No. 408

Methods link ECL and PECL

Cleon Petty and Gary Tharalson, Motorola Semiconductor, Logic IC Division, Mesa, AZ

The circuit in **Fig 1** is one way to link ECL to positive ECL (PECL). So far, no dedicated level-shifting ICs are available for these purposes.

Because the circuits in **Fig 1** are ac-coupled, you cannot use them for discontinuous data. If the inputs go quiet or are pulled high or low, the devices' differential inputs float, possibly resulting in self-oscillation.

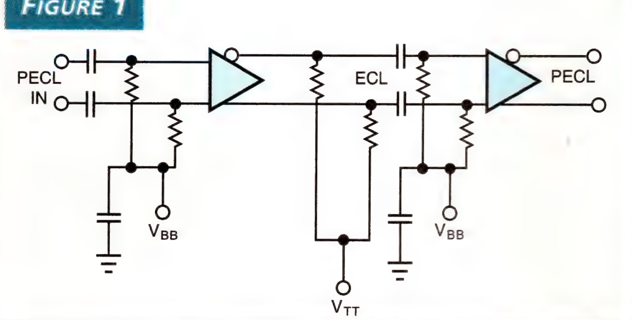
Fig 2a shows an alternative to ac coupling for ECL-to-PECL-level translation: here, an ECL MNC10116 or an MC10H116 line receiver with +5V applied to its V_{CC} pin and –5.2V applied to its V_{EE} pin. Although these devices are not specified for these voltages, testing shows the devices to be reliable when operated at these voltages.

The V_{BB} output of the 116 is referred to V_{CC}; therefore, the output is at a PECL level (V_{CC}=1.3V), which is not usable for standard ECL inputs. Consequently, you can use the 116 only for applications in which the ECL inputs are differential and not single-ended. This configuration allows an ECL-to-PECL translation at the same speed as a standard 116, although the power consumption is slightly higher. Successful translations can occur at frequencies up to 250 MHz.

Here, the V_{CC} and V_{EE} rails are at +5V and –5.2V, respectively. The PECL differential levels connect to the differential comparator's inputs, and the latch-control is high. The Q and $\overline{Q}$ outputs provide a differential ECL translation of the PECL inputs. (DI #1661) EDN

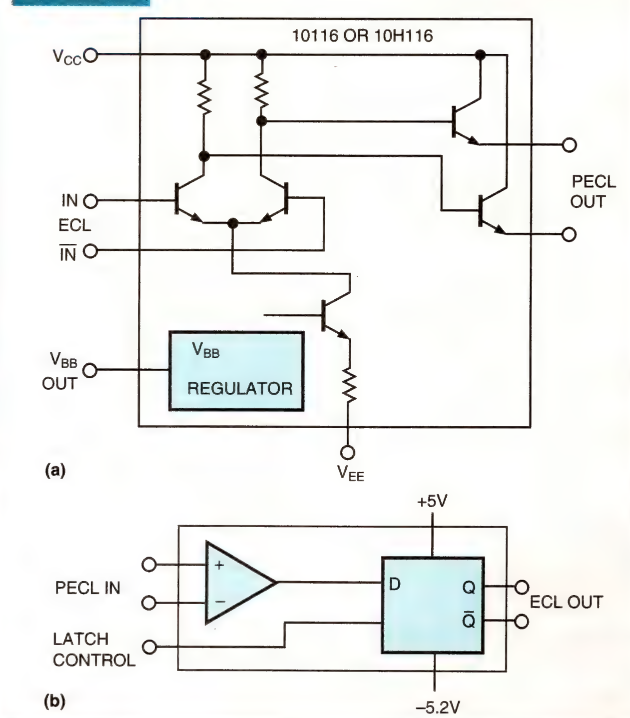
To Vote For This Design, Circle No. 409

FIGURE 1

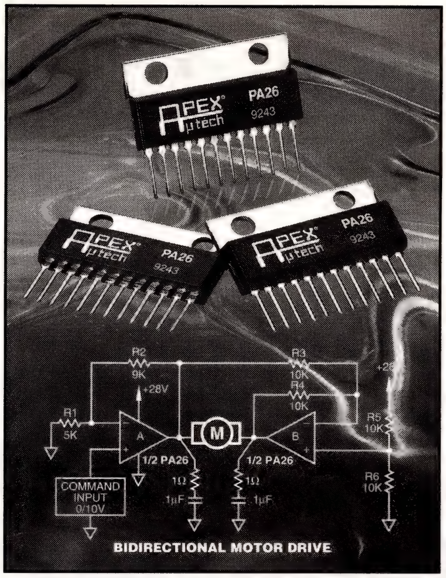


You can use these circuits to connect ECL to PECL. These ac-coupled circuits suit only continuous data.

FIGURE 2



Although ECL MNC10116 or MC10H116 line receivers are not specified for the voltages shown (a), testing shows them to be reliable when operated at these voltages for ECL-to-PECL-level translation. An MC10E/100E1651 dual analog comparator handles PECL-to-ECL translations.



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The PA26 is a low cost, 6V-40V, 3A, low VSAT, single supply power op amp. Housed in a 12-pin SIP, the PA26 makes efficient use of valuable board space. Priced $3.45 in 10K piece quantities. Typical applications: uni-or-bi-directional brush type DC motor drives, audio, linear actuator drives, and automotive controls.

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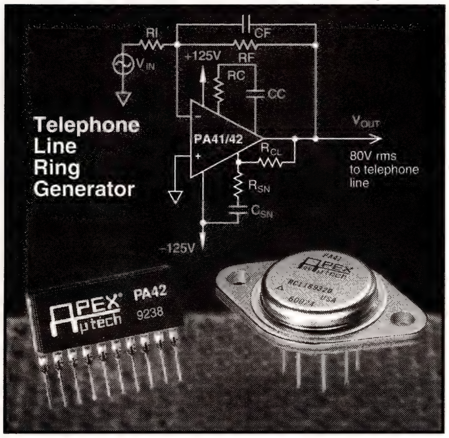

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The PA42 is the industry's first single in-line packaged (SIP) monolithic power op amp capable of operating at 350V supplies rail-to-rail. The PA42 is extremely cost effective at $17.90 in 10,000 piece quantities. Other specs include 120mA output peak, 40V/µs slew rate, MOSFET design and 2mA quiescent current. Typical applications: guidance systems and gyros, piezo drive, ATE pin drivers and deflection beam for CRT systems. The PA41 is the TO-3 packaged version of the PA42 now available in a hi-rel grade—the PA41M.

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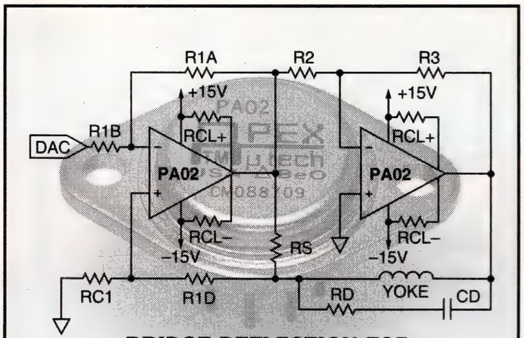

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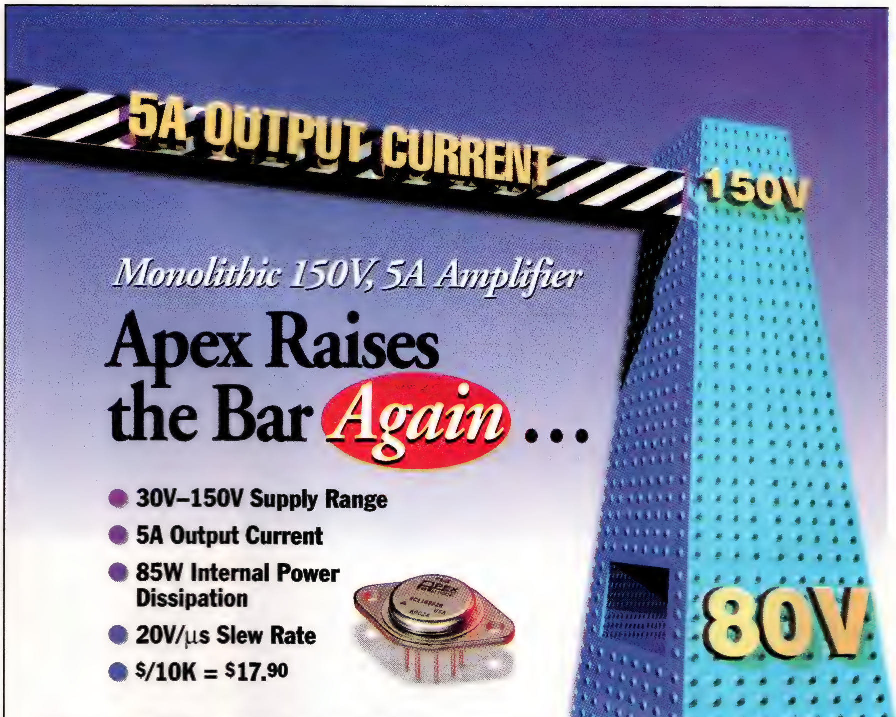

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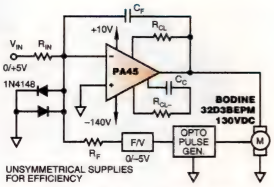

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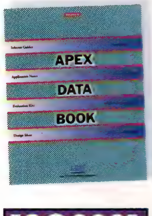

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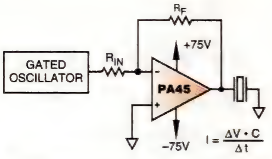

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Charge pump generates positive bias

Steve Mowry, Siemens Industrial Automation, Johnson City, TN

Placing the averaging filter inductor in the output return leg of an isolated forward-converter power supply can significantly reduce the common-mode noise the supply generates. This technique can eliminate some of the high-frequency spikes present on the output voltage. The inductor has a blocking effect on the high-frequency currents that the primary switching transistor generates. These currents flow through the transformer's stray capacitance to system ground. This configuration allows you to connect the cases of the output rectifier diodes directly to the dc output voltage and eliminates the high dV/dt normally present on the tabs. This connection prevents common-mode current flow through the isolation-barrier capacitance between the diodes' cases and the grounded heat sink.

However, this approach prevents the generation of a secondary-side bias voltage, normally accomplished by peak charging a capacitor with the voltage pulse at the input of the averaging inductor. The circuit in **Fig 1** solves this problem. An inverting charge-pump arrangement generates a positive dc bias voltage from the negative voltage pulse present on the ac side of the inductor. C_1 charges through R_1 and D_1 during the on time of the forward converter and discharges into C_2 during the flyback period. The generated bias voltage is approximately equal to V_{PEAK}(WINDING)+V_{OUT}. (DI #1664) EDN

To Vote For This Design, Circle No. 410

FIGURE 1

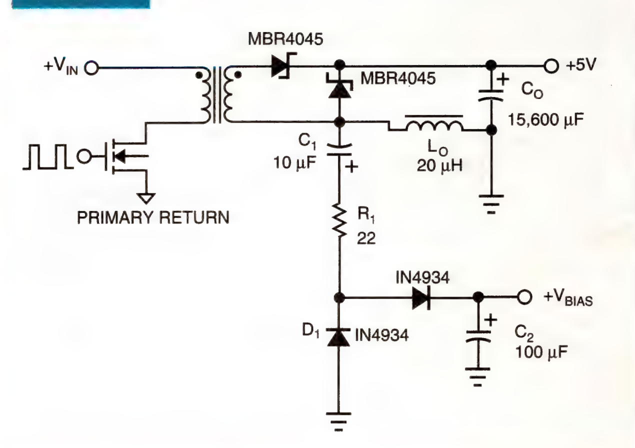


Fig 1—An inverting charge pump arrangement generates a positive dc bias voltage from the negative voltage pulse present on the ac side of the inductor.

LINEAR TECHNOLOGY

DESIGN NOTES

Highly Integrated High Efficiency DC/DC Conversion

Design Note 98

San-Hwa Chee and Howard Haensel

The LTC®1574 and LTC1265 high efficiency step-down regulators minimize external components by using integrated low RDS(ON) P-channel switches. The LTC1574 goes one step further by including a low forward drop Schottky diode—an industry first. Both regulators also include on-chip low-battery detectors.

Burst Mode™ operation allows the LTC1574 and LTC1265 to achieve over 90% efficiency for load currents as low as 10mA. Current mode operation provides clean start-up, accurate current limit, and excellent line and load regulation. Inherent 100% duty cycle in dropout allows the user to extract maximum battery life. Both regulators can be shut down to a few microamperes.

LTC1574

The LTC1574 features the highest level of integration for a switching regulator. Besides an on-chip power MOSFET, it includes a low forward drop Schottky diode. The user needs only to provide an inductor and input/output filter capacitors for a complete high efficiency step-down converter. The current limit is pin selectable to either 340mA or 600mA, optimizing efficiency for a wide range of load currents.

Figure 1 shows a typical LTC1574 surface mount application requiring only three external components. It provides 3.3V at 150mA from an input voltage of 5V. Peak inductor current is limited to 340mA by connecting pin 6 (I_{PGM}) to ground. For applications requiring higher output current, connect pin 6 to V_{IN}. Under this condition the maximum load current is increased to 425mA. Efficiency curves for the two conditions on I_{PGM} are graphed in Figure 2. Note that all components remain the same for the two curves.

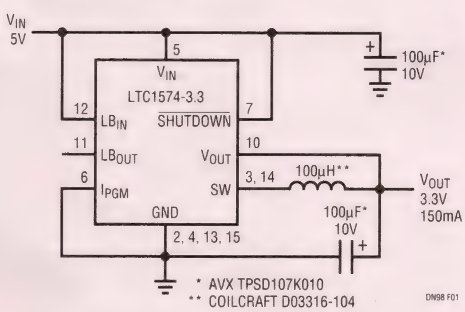


Figure 1. LTC1574 3.3V, 150mA Surface Mount

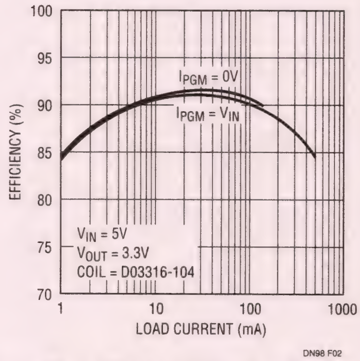


Figure 2. LTC1574 5V to 3.3V Efficiency

Low Noise Regulator

In some applications, it is important not to introduce any switching noise within the audio frequency range. Due to the Burst Mode nature of the LTC1574, there is a possibility that the regulator will introduce audio noise at some load currents. To circumvent this problem, a feed-forward capacitor can be used to shift the noise spectrum up and out of the audio band. Figure 3 shows the low noise connection with C2 being the feed-forward capacitor. The peak-to-peak output ripple is reduced to 30mV over the entire load range. A toroidal surface mount inductor L1 is chosen for its excellent self-shielding properties. Open magnetic structures such as drum and rod cores are to be avoided since they inject high flux levels into their surroundings. This can become a major source of noise in any converter circuit.

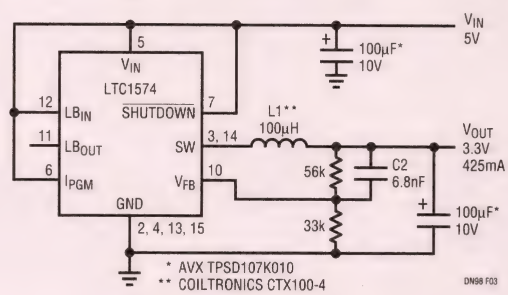


Figure 3. Low Noise 5V to 3.3V Regulator

LTC1265

Whereas the LTC1574 can only supply a load current up to 425mA, the LTC1265 can source up to 1.2A. It features a low 0.3Ω (V_{IN} = 10V) internal P-channel MOSFET to provide high efficiency at high load current. The inductor current is user-programmable via an external current sense resistor. Operation up to 700kHz permits the use of small surface mount inductors and capacitors. The LTC1265 employs an external Schottky diode.

Unlike the LTC1574 which always operates in Burst Mode, the LTC1265 only operates in Burst Mode at light loads and switches to continuous operation at heavier loads. For the LTC1265 to operate in Burst Mode, the load current has to be less than $15mV/R_{SENSE}$.

Figure 4 shows a typical LTC1265 surface mount application. It provides 3.3V at 1A from an input voltage range of 4V to 12V. Efficiency at various input voltages is plotted in Figure 5. Here the sense resistor is chosen as 0.1Ω, therefore the LTC1265 will go into continuous mode operation for load currents greater than 150mA. The peak efficiency approaches 93% at mid-current levels.

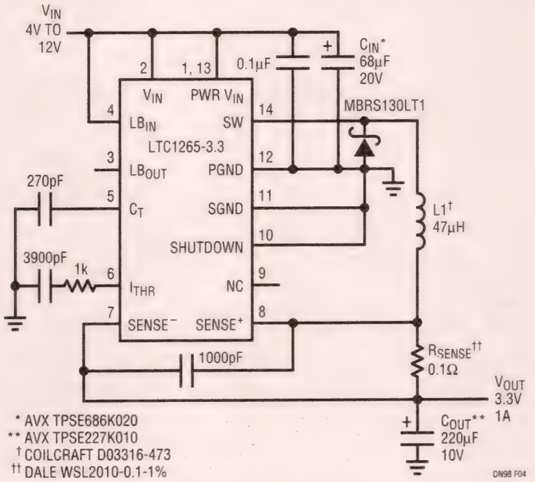


Figure 4. LTC1265 3.3V, 1A Surface Mount

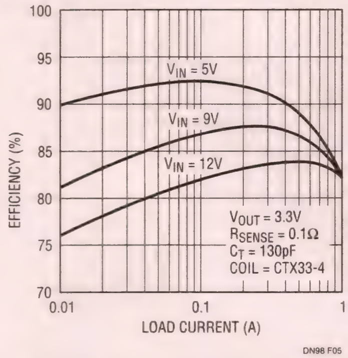


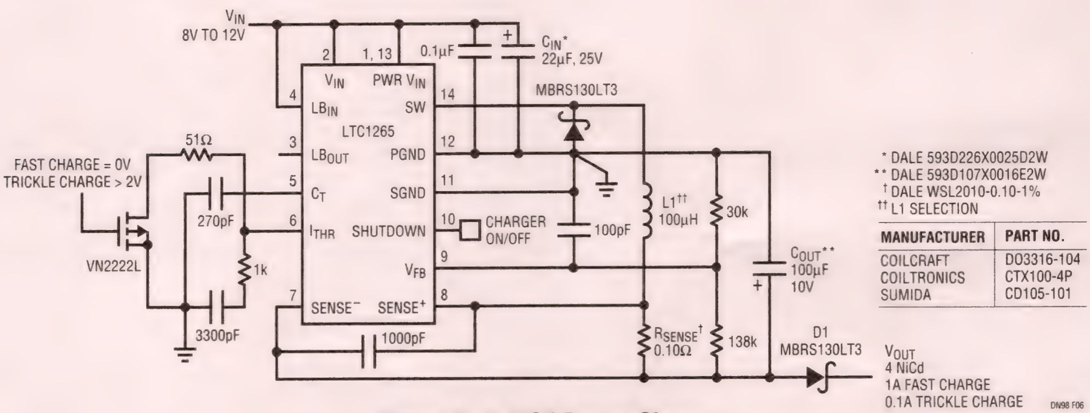
Figure 5. LTC1265 5V to 3.3V Efficiency

Battery Charger Application

In Figure 6, the LTC1265 is configured as a battery charger for a four-NiCd stack. It has the capability of performing a fast charge of 1A, a trickle charge of 100mA or the charger can be shut off. In shut-off, diode D1 serves two purposes. First, it prevents the LTC1265 circuitry from drawing battery current and second, it eliminates "back powering" the LTC1265 which avoids a potential latch condition at power-up.

LTC1574 or LTC1265?

The LTC1574 and LTC1265 are differentiated by both the output current level and operating mode. For loads less than 425mA, the LTC1574 is the ideal choice because of its simplicity and ease of use. However, for applications requiring continuous mode operation, or more than 425mA output current, the LTC1265 must be used. Both devices can be tailored to meet a wide range of requirements.



* DALE 593D226X0025D2W
** DALE 593D107X0016E2W
† DALE WSL2010-0.10-1%
†† L1 SELECTION

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Figure 6. 4 NiCd Battey Charger

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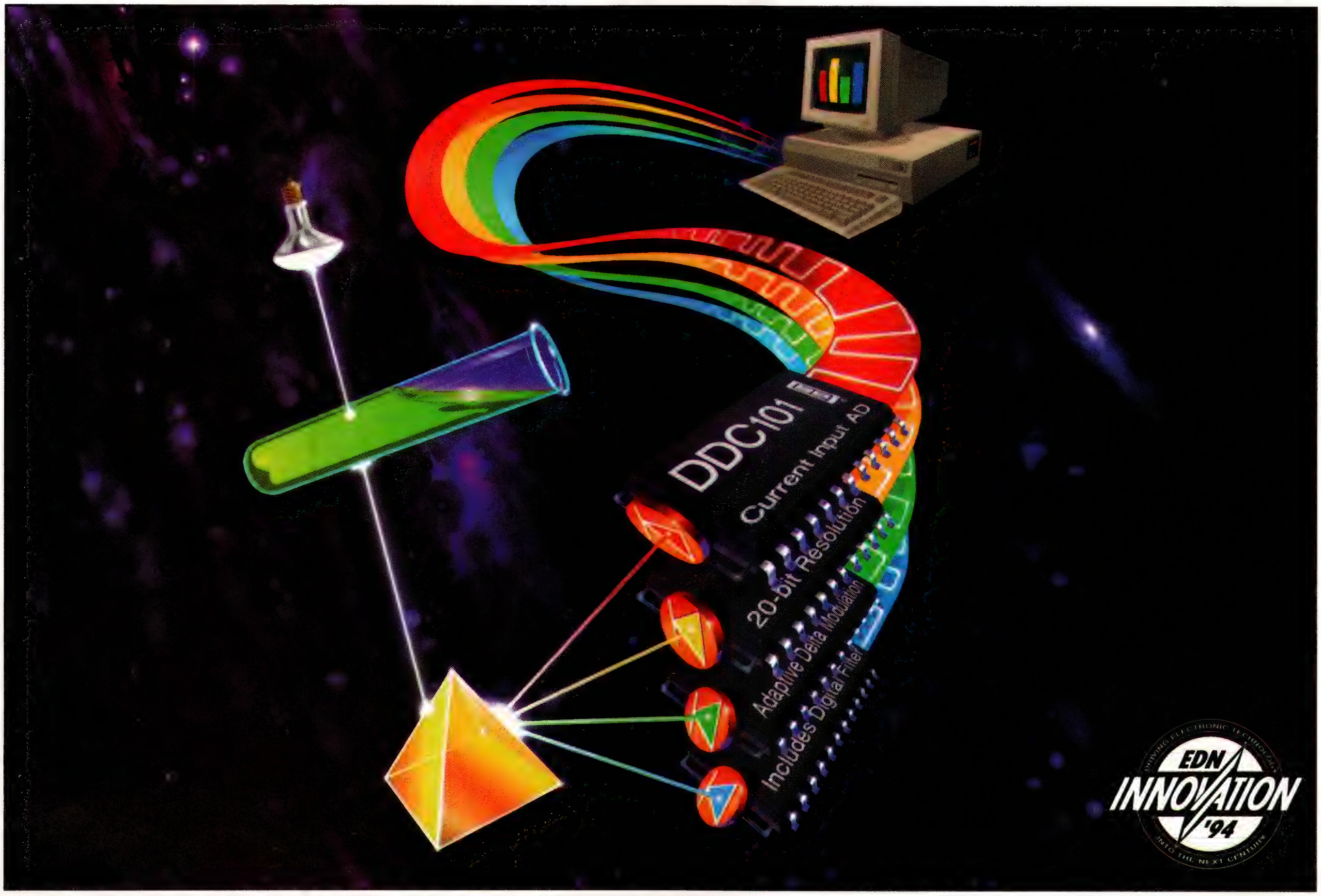

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DDC101 Key Specifications

- Resolution 20-bit
- Noise .... 1.6ppm, rms
- Conversion rate .... up to 15kHz
- Accuracy at low level .... 2.5ppm of FSR, (max)
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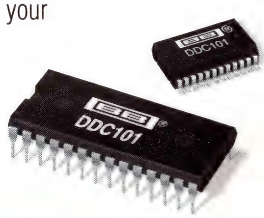

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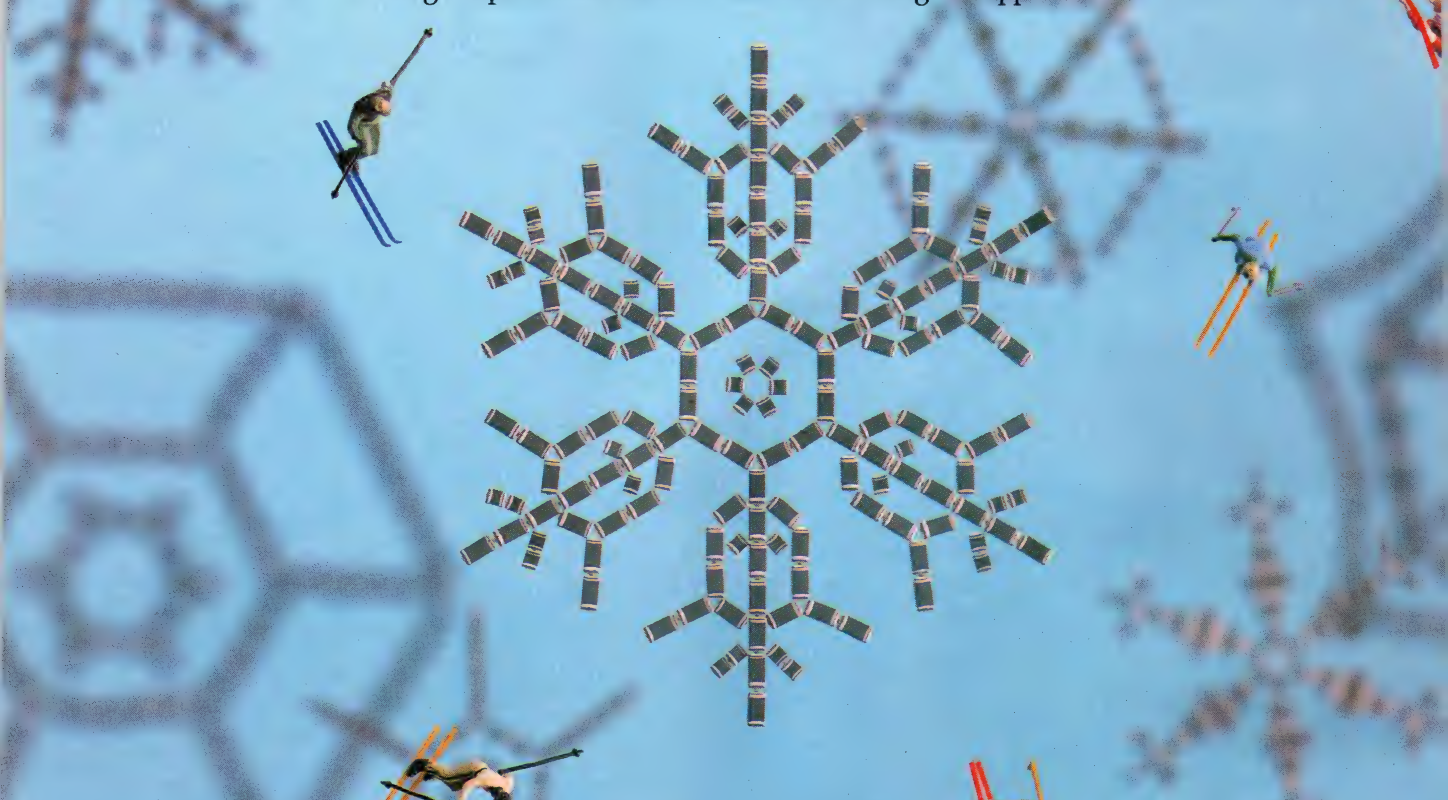

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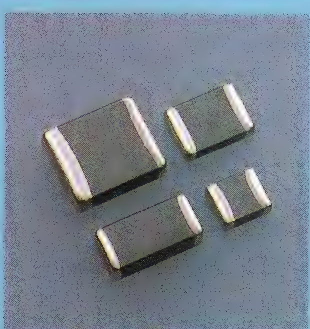

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1.5	*	*			C505
2.2		*	C304	C205	
3.3	C205*	*			
4.7	*	C304*	C505		
6.8	*	*			
10	*	*			
15	C505				
18					
22					

End terminations Fired-on end termination : All case code
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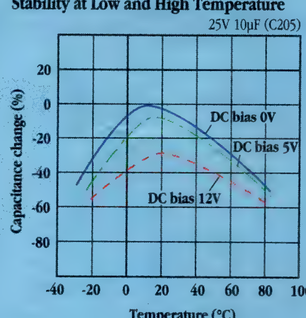

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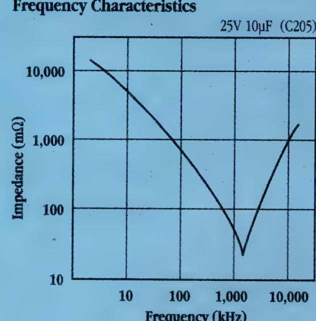

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CIRCLE NO. 163

Quaternions quickly transform coordinates without error buildup

DO-WHILE JONES

If you have data gathered in one coordinate system and want to express them in terms of a different coordinate system, you probably would use a translation vector and a rotation matrix. You can, however, use a translation vector and a quaternion instead.

Quaternions prove useful for coordinate transformations. The quaternion method is better if one of the coordinate systems keeps moving—which is the usual case in navigation and animated 3-D graphics. You can rotate a quaternion faster than you can rotate a matrix. And, unlike rotation matrices, quaternions never lose their orthogonality, which causes distortion, after many rotations.

Few people use and understand quaternions because most of the literature about quaternions involves obscure mathematical derivations and requires super-imaginary numbers that are the fourth root of –1. I will spare you all that. Instead of talking about how difficult quaternions are to derive, I will show you how easy they are to use.

A quaternion is just an ordered set of four values. You can think of it as a rotational state vector. Simple equations allow you to relate a quaternion to the corresponding rotation matrix, and vice versa.

The quaternion advantage

A quaternion doesn't have one big problem that a rotation matrix has. A rotation matrix is always overspecified. Consider a simple 2-D rotation matrix.

$$A = \begin{vmatrix} C & S \\ -S & C \end{vmatrix}$$

where $C = \text{Cos}(\Theta)$
$S = \text{Sin}(\Theta)$

Although the matrix has four elements, it has only *one* independent variable. The angle Θ completely determines all four values. You cannot, however, determine Θ uniquely from just one element of the matrix. That is, if S=0.5, you can't tell if Θ is 30 or 150°.

But, given just one row or one column of the matrix, you can determine the angle Θ if both entries are correct. For example, if S=0.5 and C=0.866, Θ must be 30 rather than 150°.

Suppose, however, an entry is in error, such that S=0.5 and C=0.857. Is the angle 30 or 31°? Representing one angle by two numbers has introduced some uncertainty. Furthermore, two of the four elements in the 2-D rotation matrix are or should be redundant. They provide no additional information when they are accurate, and they provide only confusion when they are inaccurate.

Suppose you want to find the rotation matrix for a 2-D coordinate system after rotating it clockwise 15°, then counterclockwise 5°, then clockwise 20°, and, finally, clockwise 8°. You know that Θ=–15°+5°–20°–8°=–38°. You can perform that calculation in your head. Therefore, the correct rotation matrix should have Cos(–38°) on the diagonal and ±Sin(–38°) in the other corners.

But, suppose you actually run these calculations on your computer, computing the rotation matrix for –15°, then multiplying it by the rotation matrix for +5°, then multiplying that product by the rotation matrix for –20°, and, finally, multiplying that result by the rotation matrix for –8°. Again, you *should* wind up with a rotation matrix with Cos(–38) on the diagonals and ±Sin(–38) in the corners—but will you? Will A11 be exactly equal to A22? Will A21 exactly equal –A12? Will Square_Root(A11 * A11 + A12 * A12) exactly equal 1? The answers to these questions all depend on the accuracy of the computer's arithmetic.

Even if the chain of matrix multiplications does yield the right answer, which method would you rather use: mentally adding the angular changes or multiplying the rotation matrices? The mental method involves one addition, three subtractions, one sine, and one cosine. The rotation-matrix method involves four sines, four cosines, and three matrix multiplications. So, in the 2-D case, doing the internal calculations using the first method and then converting the result to a rotation matrix is better.

The 3-D case is similar and entails three independent variables. A rotation

QUATERNIONS MADE SIMPLE

matrix maps these three variables to nine matrix elements. The 3-D matrix has added redundancy that gives you nothing but more opportunities for error than does a 2-D matrix. A quaternion, on the other hand, is a rotational state vector that maps the three independent variables into just four elements, greatly reducing the amount of redundancy.

Reducing the redundancy also reduces the number of calculations. To rotate an object, whose orientation a 3-D matrix represents, around a single axis, you must multiply that object's matrix by another rotation matrix. This procedure requires 27 multiplications, 18 additions, and three assignment operations. To rotate a quaternion about a single axis, you must multiply that quaternion by another quaternion. Quaternion multiplication takes 16 multiplications, 12 additions, and four assignments. Quaternions save 11 multiplications and six additions at the expense of one assignment operation for single-axis rotations.

When working in 3-D, you usually rotate an object about the yaw axis, then the pitch axis, and, finally, the roll axis to establish the object's new orientation. Using quaternions instead of matrices saves 33 multiplications and 18 additions for each three-axis rotation. Because time is usually critical in navigation routines and 3-D animation, saving 33 multiplications per rotation is desirable.

Any four random values—as long as all four aren't zero—create a valid rotation quaternion. This property makes the quaternion useful for generating randomly oriented test cases to test coordinate-conversion algorithms. On the other hand, any nine random values probably don't create a valid rotation matrix because certain elements of the matrix must relate to other elements in a prescribed way. Multiplying an object's orientation matrix by a random matrix not only rotates the object, but also distorts its shape.

This distortion is important because navigation and animation programs multiply the object's orientation matrix every time its position changes. It doesn't take long for the programs to multiply the matrix thousands of times. Truncation and rounding errors add a tiny bit of randomness to each element of the matrix every time the programs multiply it. Soon, the matrix is no longer perfectly orthogonal. The effect is the same as if you multiply the matrix by a random matrix—distorting the object's shape.

For several reasons, the problem is worse in a navigation routine than in a 3-D animation program. First, because navigation routines run for hours or days longer than animation routines, errors have more time to build. Second, the distortion of the "shape" of the matrix distorts the guidance commands,causing coupling. Such coupling could cause starboard-yaw commands to have the side effect of producing small counterclockwise roll commands. Third, people's lives depend on navigation routines more often than they do on animation routines. Therefore, keeping the orientation matrix orthogonal is important.

You can keep the matrix orthogonal by using double-precision arithmetic or by periodically normalizing the matrix. Unfortunately, both of these solutions take time. But, unlike matrices, quaternions never become distorted. By the way, you can easily fix a matrix that has become distorted and needs to be normalized by converting it to a quaternion and then converting the quaternion back to a matrix. I guarantee that the resulting matrix will be orthogonal.

Quaternions will never completely replace rotation matrices. The rotation matrix is unsurpassed for rotating vectors. Just multiply the matrix by the vector and get the vector result. But this facility with vectors doesn't mean you have to use the rotation matrix for *all* the intermediate transformation calculations. Computing a series of 2-D rotations as the sum of angular rotations and converting the final result to a matrix is better; computing a series of 3-D rotations using a quaternion is better, too. Do all the rotation calculations on a quaternion; then, convert the quaternion to a rotation matrix.

Quaternion/matrix conversions

The conversions between quaternions and rotation matrices are simple. Consider quaternion Q and an equivalent rotation matrix, M.

$$Q = \begin{vmatrix} Q1 \\ Q2 \\ Q3 \\ Q4 \end{vmatrix}$$

$$M = \begin{vmatrix} M11 & M12 & M13 \\ M21 & M22 & M23 \\ M31 & M32 & M33 \end{vmatrix}$$

Most mathematicians would tell you to use the following equations to convert Q to M:

$$
\begin{aligned}
M11 &= Q1^2 + Q2^2 - Q3^2 - Q4^2 \\
M12 &= 2 * (Q2*Q3 - Q1*Q4) \\
M13 &= 2 * (Q2*Q4 + Q1*Q3) \\
M21 &= 2 * (Q2*Q3 + Q1*Q4) \\
M22 &= Q1^2 - Q2^2 + Q3^2 - Q4^2 \\
M23 &= 2 * (Q3*Q4 - Q1*Q2) \\
M31 &= 2 * (Q2*Q4 - Q1*Q3) \\
M32 &= 2 * (Q3*Q4 + Q1*Q2) \\
M33 &= Q1^2 - Q2^2 - Q3^2 + Q4^2
\end{aligned}
$$

These equations assume that quaternion Q has been normalized. If Q is not normalized, you must divide each of the elements by $Q1^2 + Q2^2 + Q3^2 + Q4^2$.

These equations aren't difficult to compute as they stand, but clever collection of terms in five temporary variables (TX, TY, TZ, TQ and TK) can further reduce computation time. **Algorithm 1** is a better way to convert a quaternion to a matrix.

Algorithm 1

```
TX  = Q2*Q2
TY  = Q3*Q3
TZ  = Q4*Q4
TQ  = TY+TZ
if (TQ + TX + Q1*Q1) is not 0 then
TK = 2 / (TQ + TX + Q1*Q1)
else
 TK  = 0
M11 = 1 - TK*TQ
M22 = 1 - TK*(TX + TZ)
M33 = 1 - TK*(TX + TY)
TX  = TK*Q2
TY  = TK*Q3
TQ  = (TK*Q4)*Q1
TK  = TX*Q3
M12 = TK - TQ
M21 = TK + TQ
TQ  = TY*Q1
TK  = TX*Q4
M13 = TK+TQ
M31 = TK-TQ
TQ  = TX*Q1
TK  = TY*Q4
M23 = TK - TQ
M32 = TK + TQ
```

Algorithm 1 normalizes the quaternion as a natural side effect of the col-

QUATERNIONS MADE SIMPLE

lection of terms, so you need not normalize Q before converting it to a rotation matrix. You don't need to normalize quaternions before multiplying them, so, if you use **Algorithm 1** to convert a quaternion to a matrix, you need not normalize quaternions. Omitting the unnecessary normalization saves time.

You can convert M to Q in any of four easy ways. Some ways work better than others for certain situations. The conversion is much like computing an arctangent. You can write a series that computes the arctangent of Y/X. The series converges rapidly when X is much larger than Y, but it takes a long time to converge when X is small, especially when X is 0. Therefore, good arctangent routines take advantage of the fact that arctangent (Y/X)=90°– arctangent(X/Y). Good arctangent routines use the alternate form whenever Y>X. Good arctangent routines also use tricks to fold angles from the second, third, and fourth quadrants into the first quadrant before computing the result, and the routines then adjust the result based on the quadrant.

Algorithm 2 selects one of the four matrix-to-quaternion conversion routines, depending on the values on the diagonal of the rotation matrix.

Algorithm 2

```
if M11 ≥ 0 and (M22 + M33) ≥ 0 then
    Q1=  1 + M11 + M22 + M33
    Q2=  M32 – M23
    Q3=  M13 – M31
    Q4=  M21 – M12

if M11 ≥ 0 and (M22 + M33) 0 then
    Q1=  M32 – M23
    Q2=  1 + M11 – M22 – M33
    Q3=  M21 + M12
    Q4=  M13 + M31

if M11 0 and (M22 - M33) ≥ 0 then
    Q1=  M13 – M31
    Q2=  M21 + M12
    Q3=  1 – M11 + M22 – M33
    Q4=  M32 + M23

if M11 0 and (M22 – M33) 0 then
    Q1=  M21 – M12
    Q2=  M13 + M31
    Q3=  M32 + M23
    Q4=  1 – M11 – M22 + M33
```

Quaternion multiplication

Just as you can multiply two rotation matrices to get another rotation matrix, you can multiply quaternions to compute the effect of a series of rotations. Like matrix multiplication, quaternion multiplication is not commutative because the order of rotation matters. To see why the order matters, imagine an airplane pointing north. If you rotate it 90° to its right, it will be pointing east. If you then pitch it up 90°, it will be standing on its tail. But if you take an airplane pointing north, pitch it up 90°, and then rotate it to its right 90°, it will wind up standing on its starboard wing tip.

Let's define three quaternions to have elements Q, L, and R:

$$Q = \begin{matrix} Q1 \\ Q2 \\ Q3 \\ Q4 \end{matrix} \qquad L = \begin{matrix} L1 \\ L2 \\ L3 \\ L4 \end{matrix} \qquad R = \begin{matrix} R1 \\ R2 \\ R3 \\ R4 \end{matrix}$$

To compute the quaternion product Q=L*R, use **Algorithm 3**:

Algorithm 3

```
Q1  =  L1 * R1 – L2 * R2 – L3 * R3 – L4 * R4
Q2  =  L2 * R1 + L1 * R2 – L4 * R3 + L3 * R4
Q3  =  L3 * R1 + L4 * R2 + L1 * R3 – L2 * R4
Q4  =  L4 * R1 – L3 * R2 + L2 * R3 + L1 * R4
```

Algorithm 3 uses 16 multiplications and 12 additions. In comparison, it takes three multiplications and two additions to compute each of the nine elements in a 3-D rotation matrix. Thus, using quaternions saves 11 multiplications, six additions, and five assignment statements. These savings mean that you can multiply quaternions in roughly half the time multiplying rotation matrices takes.

Rotating quaternions

A quaternion rotates an object an angle Θ about an axis. Let Ai + Bj + Ck be a unit vector outward from the origin representing an axis of revolution. Let Θ represent the (right-handed) angle of rotation about that axis. **Algorithm 4** shows how to find the quaternion that produces this rotation.

Algorithm 4

```
Q1=       Cos(Θ / 2)
Q2=  A *  Sin(Θ / 2)
Q3=  B *  Sin(Θ / 2)
Q4=  C *  Sin(Θ / 2)
```

Rotating an object using a series of three rotations is common practice. First, rotate the object in the yaw direction. Second, rotate it in the pitch plane. Third, rotate it around the roll axis. In these cases, the unit vector along the rotation axis aligns with a coordinate axis, so two of the three components, A, B, and C, are zero, and the remaining component is plus or minus one. **Algorithm 4** degenerates to the following three special cases.

Algorithm 4a

To rotate in the yaw direction:

```
Q1 = Cos(Θ / 2)
Q2 = 0
Q3 = 0
Q4 = –Sin(Θ / 2)
```

Algorithm 4b

To rotate in the pitch direction:

```
Q1 = Cos(Θ / 2)
Q2 = Sin(Θ / 2)
Q3 = 0 Q4 = 0
```

Algorithm 4c

To rotate in the roll direction:

```
Q1 = Cos(Θ / 2)
Q2 = 0
Q3 = Sin(Θ / 2)
Q4 = 0
```

Rotation rates

Calculations often yield the rotation rates about the three axes. Although the order of rotation is important in theory, the rotation order does not matter much in practice if the magnitude of the rotation is small. Therefore, if rates are in radians per second, and DELTA_T is a small value (seconds), **Algorithm 5** can compute the new orientation of the quaternion, Q.

Algorithm 5

```
Y  =  YAW_RATE * DELTA_T
P  =  PITCH_RATE * DELTA_T
R  =  ROLL_RATE * DELTA_T

T  =  1 – (R*R + P*P + Y*Y) / 12
T1 =  Q1*T – (R*Q2 + P*Q3 + Y*Q4) / 2
T2 =  Q2*T + (R*Q1 – P*Q4 + Y*Q3) / 2
T3 =  Q3*T + (R*Q4 + P*Q1 – Y*Q2) / 2

Q4 = Q4*T + (–R*Q3 + P*Q2 + Y*Q1) / 2
Q3 = T3
Q2 = T2
Q1 = T1
```

This second-order approximation is accurate to 1 sec of error when the values of Y, P, and R are less than 0.17 radians (10°). When you write the code, multiply by the reciprocals of the constants because multiplication is faster than division.

If a quaternion, Q, represents the current orientation of an object and if you want small angles Y, P, and R to

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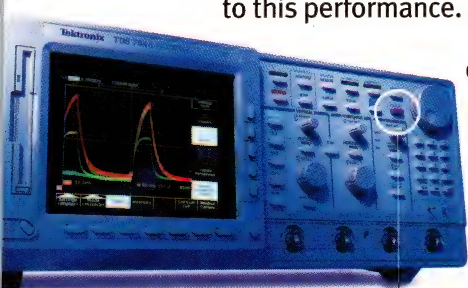

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rotate the object (in radians), computing the quaternion's new orientation takes only 24 multiplications, 15 additions, and *no* sines or cosines. That calculation is much faster than the 81 multiplications and 54 additions multiplying an orientation matrix by three rotation matrices would take—and that isn't counting the three sines and three cosines you would have to compute to create the three rotation matrices.

The derivations of these simple algorithms are complex. Those complex, inscrutable derivations tend to scare people away from quaternions. Fortunately, you don't need to derive the equations every time you use these algorithms. Just pretend they are matrix operations optimized for speed, with the fortunate side effect of keeping the matrix orthogonal after every multiplication. EDN

Acknowledgment

David A Scott of Ridgecrest, CA, did the work that is the basis for this article. He developed the improved algorithms for converting between quaternions and rotation matrices.

Author's biography

Do-While Jones is a software engineer who has worked for the defense industry of a free-world nation since 1971. He has obtained a patent for a radar signal-processing algorithm and has an EE degree. The author of the book Ada in Action, *he has published more than 40 articles in popular computer magazines. You may contact him at do_while@ridgecrest.ca.us on the Internet.*

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DK Mer-el A/S, Tel. 0045-42-571000, Fax 0045-42-572299
DK Peter Petersen A/S, Tel. 0045-86-836211, Fax 0045-86-836383
TR Empa Electronik A.S., Tel. 0090-212-5993050, Fax 0090-212-5985353
IL Rakon Components, Tel. 0097-236951055, Fax 0097-236951743

SHARP ELECTRONICS (EUROPE) GMBH
Microelectronics Division (MED)
Sonninstraße 3, 20097 Hamburg
Phone +49-40/2376-2286, Telex 2 161 867
Telefax +49-40/2376 22 32

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SHARP offers a wide range of active and passive colour, passive monochrome LCDs and Electro-Luminescent Displays from 3" (7,6 cm) upto 14,2" (36 cm) in size which are in production.

SHARP has also successfully demonstrated a 17" (43 cm) TFT-Display for workstation with 1280 x 1024 resolution and completed development of a 21" (53 cm) multi-media compatible TFT Display with 16,7 million colours.

SHARP

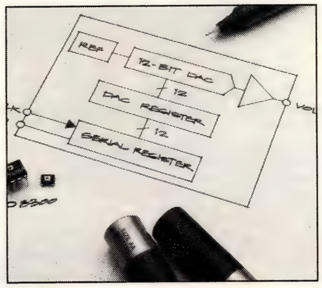
THE IDEAS COMPANY

Opti Inc, Santa Clara, CA. (408) 980-8178.
Circle No. 416

900-MHz, unity-gain-stable op amp has low power dissipation and low price. The OPA658 current-feedback op amp offers a high bandwidth yet dissipates 50 mW and costs $2.25 (1000). Operating from ±5V supplies, the op amp offers a 68-dBc spurious-free dynamic range) at 5 MHz, a 1700-V/µsec slew rate, and a 0.025%/0.02° differential gain/phase error. **Burr-Brown Corp**, Tucson, AZ. (602) 746-1111.
Circle No. 417

Two-chip set integrates speaker phone, digital answering machine, and facsimile modem. The RFX96V12-S sends and receives Group 3 facsimiles at 14.4 to 24 kbps with V.23 full-duplex support. The digital answering machine allows 12 minutes of voice storage in 4 Mbits of RAM. The chip set comprises a 100-pin PQFP and a 28-pin PLCC. $38 (10,000). **Rockwell Telecommunications**, Newport Beach, CA. (800) 436-9988. **Circle No. 418**

MPEG decoder for PCs provides glueless support for ISA, VL, and PCI interfaces. The OTI-201 decoder supports MPEG 1 and MPEG 2, main-profile, low-level bit streams. The MPEG 2 6-Mbps capability typically lets you take advantage of 2X and 4X CD-ROM drive technology. The decoder works with the company's video and graphics accelerator to provide all functions on a single board. The chip costs $29 (10,000). **Oak Technology Inc**, Sunnyvale, CA. (408) 737-0888.
Circle No. 419



12-bit voltage-output DAC operates from single 3V supply. The AD8300 integrates a converter, a reference, and an output amplifier in an SO-8 or eight-pin DIP package and requires no external components. The converter provides 0.5 mV/bit (2.0475V full scale). The output amplifier can swing to either supply rail and sources or sinks up to 5 mA. Operating voltage is from 2.7 to 5.5V. $4.41 (1000). **Analog Devices Inc**, Wilmington, MA. (617) 937-1428. **Circle No. 420**

Motor controller reduces ac induction motors' power consumption by 30% (typ). The MTE1122 Energy Management Controller digitally monitors the motor load and controls the power consumption thousands of times per second to match actual system requirements more accurately. (Most ac i856 induction motors require high current under light and even no-load conditions.) The controller monitors the ac signal and senses when the motor is consuming more power than is required. The device modifies the ac signal, allowing the motor to continue its

rotational speed while consuming less power. Available in an 18-pin DIP or SOIC package, the controller costs $7.49 (1000). **Microchip Technology Inc**, Chandler, AZ. (602) 786-7200.

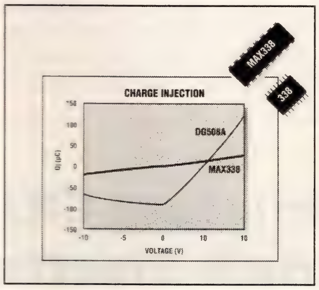
Circle No. 421

Single-chip NT-1 transceiver for ISDN. The T7256 implements an entire NT-1 interface between Integrated Services Digital Network (ISDN) lines and premises equipment. The chip complies with all European Telecommunications Standards Institute and ANSI requirements defining the standard network termination. The four major on-chip interfaces include a standard two-wire U-interface (2B1Q), the four-wire S/T interface, a serial µP interface, and a time-division-multiplexed interface allowing access to 2B+D data. The 44-pin PLCC dissipates 270 mW when active and 35 mW in idle mode. $23.90 (10,000). **AT&T Microelectronics**, Allentown, PA. (800) 372-2447. **Circle No. 422**

Design kit for Ethernet PCMCIA cards. With the 78Q8373-DB Ethernet Design Kit, you can design and build a PCMCIA Ethernet card using the company's 78Q8373 PCMCIA IC. The kit comes with a fully functioning PCMCIA Ethernet card having 32 kbytes of buffer SRAM and a 10BaseT cable connection. $199. **Silicon Systems**, Tustin, CA. (714) 573-6200.

Circle No. 423

Analog multiplexers offer low leakage and low on-resistance. The MAX338 8:1 multiplexer and the MAX339 dual 4:1 multiplexer have on- and off-channel leakage of <20 pA at 25°C. They have a maximum on-resistance of 400Ω and a charge injection of 5 pC (1.5



pC typ). ESD protection is >2000V. The multiplexers operate from a 4.5 to 30V single supply or from a ±4.5 to ±20V dual supply. Address and control inputs are TTL-compatible. The devices are pin-compatible upgrades for the industry-standard DG508A and DG509A devices. From $2.39 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600 x6087.

Circle No. 424

DSP provides single-chip implementation of the G.728 speech-compression/decompression algorithm. Operating on the 16-bit ADSP-2171 DSP, the algorithm is available in software for RAM-based systems or as a mask-programmed implementation. There are no up-front licensing fees, and the DSP with G.728 codes sells for <$20 in OEM volumes. **Analog Devices Inc**, Wilmington, MA. (617) 937-1428.

Circle No. 425

Wide-input step-down switching regulator has high efficiency. The LTC1159 synchronous regu-

lator accepts 4 to 40V input voltages and is available with a fixed 3.3V output or a programmable 5V output. For a 10V input and a 5V output, the regulator provides 90 to 95% efficiency for 20-mA to 2A currents. The regulator drives two complementary MOSFETs at switching frequencies up to 250 kHz. Quiescent current is 250 μA, and a shutdown mode reduces current to 20 μA. Dropout voltage is typically 200 mV with a 1A output current. From $4.70 (1000). **Linear Technology Corp**, Milpitas, CA. (408) 432-1900.
Circle No. 426

Video accelerator provides free MPEG-decoding technology. The Video Power video coprocessor and the company's Power 9100 64-bit graphics accelerator provide high-quality graphics. The company now offers MPEG-decompression technology licensed from Xing Technology Corp free to OEM users of the video coprocessor. The video coprocessor costs $25 in volume. **Weitek Corp**, Sunnyvale, CA. (408) 738-8400. **Circle No. 427**

800-mA low-dropout regulators are available with fixed and programmable outputs. The REG1117 has a 1.2V max dropout voltage, an internal thermal limit, and thermal-overload protection. Programmable-voltage versions require two external resistors. The device comes in an SOT-223 package and costs $1.50 (10,000). **Burr-Brown Corp**, Tucson, AZ. (602) 746-1111. **Circle No. 428**

Low-dropout-voltage regulator fits in five-pin SOT-23 package. The LP2980 has a dropout voltage of 120 mV at 50 mA and 7 mV at 1 mA. Current requirements for the device are 375 μA at 50-mA output and 80 μA at 1-mA output. Shutdown current is 1 μA max. The device comes in 3, 3.3, and 5V versions starting at $0.77 (1000). **National Semiconductor Corp**, Santa Clara, CA. (800) 272-9959. **Circle No. 429**

1.6-GHz PLL frequency synthesizer draws <0.5W. The Q3216 single-chip frequency synthesizer suits use in frequency-hopping radios, digital modems, test equipment, and local oscillators. The 44-pin PLCC package requires a single 5V supply and operates from –45 to +85°C. From $36 (1000). **Qualcomm Inc**, San Diego, CA. (619) 587-1121. **Circle No. 430**

24-bit hard-wired filter offloads dedicated filtering from DSPs for greater throughput. The HSP43124 uses 32-bit coefficients to preserve 100-

CEIBO
Development Tools of Choice

DS-186 In-Circuit Emulator

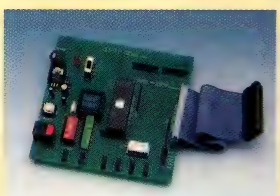
DS-186 real-time emulator supports microprocessors of the 80C186 family. The emulated devices are 80C186/8/XL/EA/EB/EC, V40/50, 8086/8 and more. The selection of a different microprocessor is made by replacing the microprocessor in the adapter or changing the adapter. The system features Full Speed Emulation up to 30MHz, 1 Mbytes of Zero Wait-State Mapped Memory, 8K Frames Dynamic Trace Buffer, 1M Hardware Breakpoints and 115KBaud RS-232C Communication Link. Breakpoints are qualified by instruction fetch, instruction execution, data contents, read/write from/to memory and I/O. The Trace display shows source, assembler and bus cycles. The system runs at the frequency of the crystal on the adapter or from the clock source supplied by the user hardware. The software supplied as standard is Paradigm Debug and Locate.

DS-51 Microprocessor Development System

Ceibo DS-51 is a real-time in-circuit emulator dedicated to the 8051 family of microcontrollers. It is serially linked to an IBM PC or compatible host and carries out a transparent emulation on the target microcontroller. DS-51 supports the new low-power and low-voltage 8051 microcontrollers and derivatives. The system can emulate the microcontrollers using either the built-in 5V power supply or any voltage applied to the target circuitry. This selection is done by means of software control. The permitted voltage range is from 1.5V to 6V or higher. DS-51 emulates almost every 8051 derivative in the complete voltage and frequency range specified by the microcontroller manufacturer. The minimum frequency is determined by the emulated chip characteristics, while maximum frequency is up to 40MHz. The software includes Source Level Debugger for PLM and C, Assembler Debugger, Performance Analyzer, On-line Assembler and Disassembler, Conditional Breakpoints and many other features. Standard systems are supplied with 128KBytes of Internal Memory, 64K Hardware Breakpoints, 32K Real-Time Trace Memory and personality probe supporting most of the 80C51 microcontrollers.

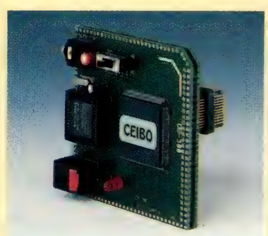
Development Tools

Ceibo offers a broad line of dedicated Development Tools for emulating different Microcontrollers and including all the necessary elements to design your embedded system. Among these tools are DB-51, DB-501, EB-51, DS-750 and DS-752.



DS-300 PSD Emulator

DS-300 is a complete software and hardware development tool that allows file generation and emulation of the PSD-3xx devices. The emulator provides an immediate way to check that the devices are properly configured and allows examination and modification of the memories and I/O lines. The configuration software provides all the elements necessary to set the device with minimum learning time.



MP-51 - Programmer

Ceibo MP-51 is a high-quality Microcontroller, Flash Memory, EPROM and PLD Programmer dedicated to all the microcontrollers belonging to the 8051 family, 24 to 32-pin EPROMs, high-density PLDs and PSD devices. MP-51 allows to enable or disable the PLD or Microcontroller security capabilities and handles Lock Bits and Encryption Table available in several Microcontrollers. MP-51 loads different file formats: Intel Hex, Intel OMF, Binary, Motorola S-records, etc. Adapters are available for all the possible packages, such as DIP, LCC, PLCC, SO, and QFP.

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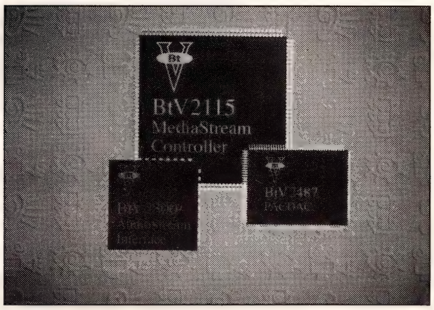
CIRCLE NO. 203

dB input dynamic range. The device mixes the digitized 8- to 24-bit input signals with external values or taken from an internal look-up table. After mixing, the device provides baseband filtering with a user-selectable cascade of up to five half-band filters, each of which decimates by 2, followed by a programmable FIR filter. The FIR filter has up to 256 taps and allows decimation by 1 to 8. Maximum clock rate for the filter is 45 MHz. The device comes in a 28-pin PDIP or an SOIC package and costs $19.94 (1000). **Harris Semiconductor**, Melbourne, FL. (800) 442-7747, ext 7294. **Circle No. 431**

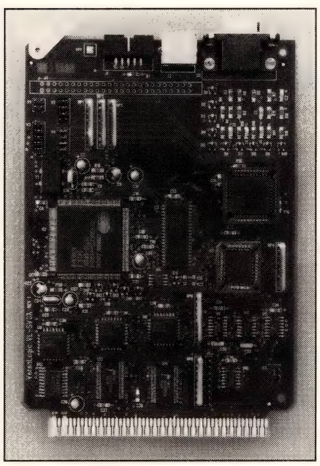


Local-bus-based media-accelerator chip set provides 1280×1024-pixel graphics at 30 frames/sec. The BtV MediaStream accelerator chip set provides high-performance graphics, DOS-games-compatible 16-bit audio or full-digital sound plus TV-quality video windows. The three-chip set uses a packet-based multimedia-handling architecture, a 1-Mbyte frame buffer, a suite of software drivers, and a connection to the Peripheral Component Interconnect or VL bus. Samples are available now, and production quantities will be available in the second quarter. **Brooktree Corp**, San Diego, CA. (619) 452-7580. **Circle No. 432**

GUI accelerator for Samsung's Window RAM. The TGUI9660XGi is a 64-bit graphical-user-interface (GUI) accelerator for the dual-ported KM4232W259 Samsung Window RAM. According to the company, the combination offers better performance and lower cost than do conventional VRAM-based graphics controllers. The chip provides a 560-Mbyte/sec bandwidth for the combined task of drawing and display. The IC comes in a 208-pin PQFP and costs $27 (10,000/month). **Trident Microsystems Inc**, Mountain View, CA. (415) 691-9211. **Circle No. 433**

Software-programmable battery-management IC accommodates rechargeable batteries. The LTC1325 IC charges various battery chemistries, including NiCd, nickel-metal-hydride, sealed lead-acid, lithium-ion, and zinc-air. The 18-pin DIP or SOIC package contains a programmable PWM constant-current switching regulator, a 10-bit A/D converter, a programmable battery-voltage divider, an internal timer, battery fault-sensor interfaces, a current monitor (gas gauge), a battery-discharge controller, and a serial interface to the system microcontroller. The device has five modes of operation: charge, discharge, gas gauge, idle, and shutdown. $6.80 (1000). **Linear Technology Corp**, Milpitas, CA. (408) 432-1900. **Circle No. 434**

Ada compiler supports Intel and Pentium processors. The DDC-I Ada compiler system provides full 486 support, including the EX, DX2, and DX4 processors. Several memory models are available, including a flat model, which improves system performance 10 to 20%, according to the company. Targeting safety-critical real-time software applications, the product provides >200 enhancements over the company's previous product. From $24,500. **DDC-I Inc**, Phoenix, AZ. (602) 275-7172. **Circle No. 474**



Industrial SVGA card with keyboard controller for STD/STD-32-bus applications. The 4.5×6.5-in. VL-SVGA-1 board is PC-software-compatible and VGA-compatible with any CRT or flat-panel display using a standard VGA connector. The board is also VESA-software-compatible and includes an onboard VGA BIOS and a standard AT keyboard controller. Maximum resolution is 1024×768 pixels with 16 colors and 800×600 or 640×480 pixels with 256 colors. $450. **VersaLogic Corp**, Eugene, OR. (800) 824-3163. **Circle No. 475**

Shareware utility library for C/C++ has nearly 1700 programs. The C/C++ utility library is available on CD-ROM ($59.50) or compressed on 99 1.44-Mbyte diskettes ($149). The library comes with an indexed database that describes all products in the library and >300 commercial products. The directory lists more than 110 types of programs. **EMS Professional Shareware**, Olney, MD. (301) 924-3594. **Circle No. 476**

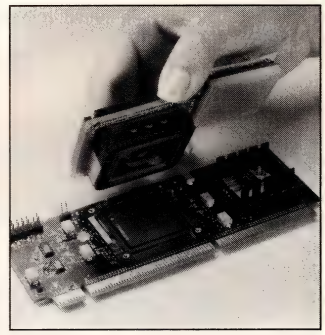
Binary-mode compiler and simulator provide 8051-to-MCS 251 migration. The ANSI C-based Starter Pack provides direct migration of 8051 applications to the faster MCS 251 architecture. The compiler requires no C or assembly-language changes to take advantage of the new microcontroller's performance. The software runs on PCs and costs $395. **Boston Systems Office/Tasking**, Dedham, MA. (617) 320-9400. **Circle No. 477**

Windows-based neural-network software package adds Kohonen algorithm. The NeuDesk neural-network software package now implements Kohonen's concept of competitive learning, allowing the network to adapt automatically and to discover patterns and associations in data without supervision. The algorithm does not require users in training to provide correct answers. The new algorithm costs $50 when purchased with the $385 NeuDesk package. **Neural Computer Sciences**, Totton, UK. +44 (0) 1703 667775. **Circle No. 478**

Flash disk comes in PC/104 form factor. The PC Flash Disk meets all standards of the PC/104 consortium and measures 3.6×3.8 in. The device is available with 1 to 32 Mbytes of memory and provides full disk emulation. The onboard expansion BIOS enables cold booting. A 1-Mbyte version starts at $99.95, and a 32-Mbyte version costs $1000 in moderate OEM volumes. **M-Systems Inc**, Santa Clara, CA. (408) 654-5820. **Circle No. 479**

ISA bus board offers two TMS320C31 floating-point DSPs. The PC-C31 Aruba offers ISA and EISA bus compatibility. It includes 2 Mbytes of zero-wait-state SRAM and two high-speed, buffered RS-422 ports, which are an extension of each of the TMS-320C31's serial ports. The device has 8 kbytes of memory-mapped dual-port RAM to facilitate interprocessor communications. Each DSP can access this memory with one wait state without interference from either the host or the other DSP. Each processor also shares a 4-kbyte, dual-port RAM bank with the host. Development support for the board includes an ANSI C compiler, an assembler, a linker, and the company's AXDS-PC-C31 emulator. With two processors and 2 Mbytes of memory, the board costs $2495. **Ariel Corp**, Highland Park, NJ. (908) 249-2900. **Circle No. 480**

VMEbus board offers high performance with microSPARC-II CPU. The single-board CPU-5V uses a 110-MHz microSPARC-II and delivers 76 SPECint92 and 65 SPECfp92. The board has a sustained VME transfer rate of over 40 Mbytes/sec, enabling it to transfer full-frame color video or graphics at 30 frames/sec. The board maintains full SPARCstation 5 compatibility and accommodates up to 192 Mbytes of onboard memory. The single 6U VME board provides a suite of workstation-compatible I/O interfaces, including Ethernet, fast SCSI-2, a parallel port, two serial ports, and a keyboard/mouse port. Two SBus slots provide I/O expansion. The board with 16 Mbytes of DRAM costs $7995. **Force Computers Inc**, San Jose, CA. (408) 369-6000. **Circle No. 481**



µP-specific and general-purpose probe adapters suit logic analyzers and oscilloscopes. Nine probe adapters interface the company's logic analyzers and oscilloscopes to 0.5- and 0.65-mm-pitch PQFP and CQFP surface-mount devices. The probe adapters require a 6-mm clearance around the perimeter of the chip. You can use two types of locator bases with the adapters to provide quick and accurate mounting of the probe to the pc board. Prices for the probe adapters range from $150 to $2400. **Hewlett-Packard Co**, Santa Clara, CA. (800) 452-4844, ext 8980. **Circle No. 482**

Mobile PCs provide data acquisition in harsh industrial environments. The 7108 mobile field computer and the 7010 ruggedized dc-powered portable field computer operate with standard software and plug-in cards. The water-resistant devices withstand temperature fluctuations, vibration, and other harsh environmental conditions. Both models can operate from batteries or ac power. From

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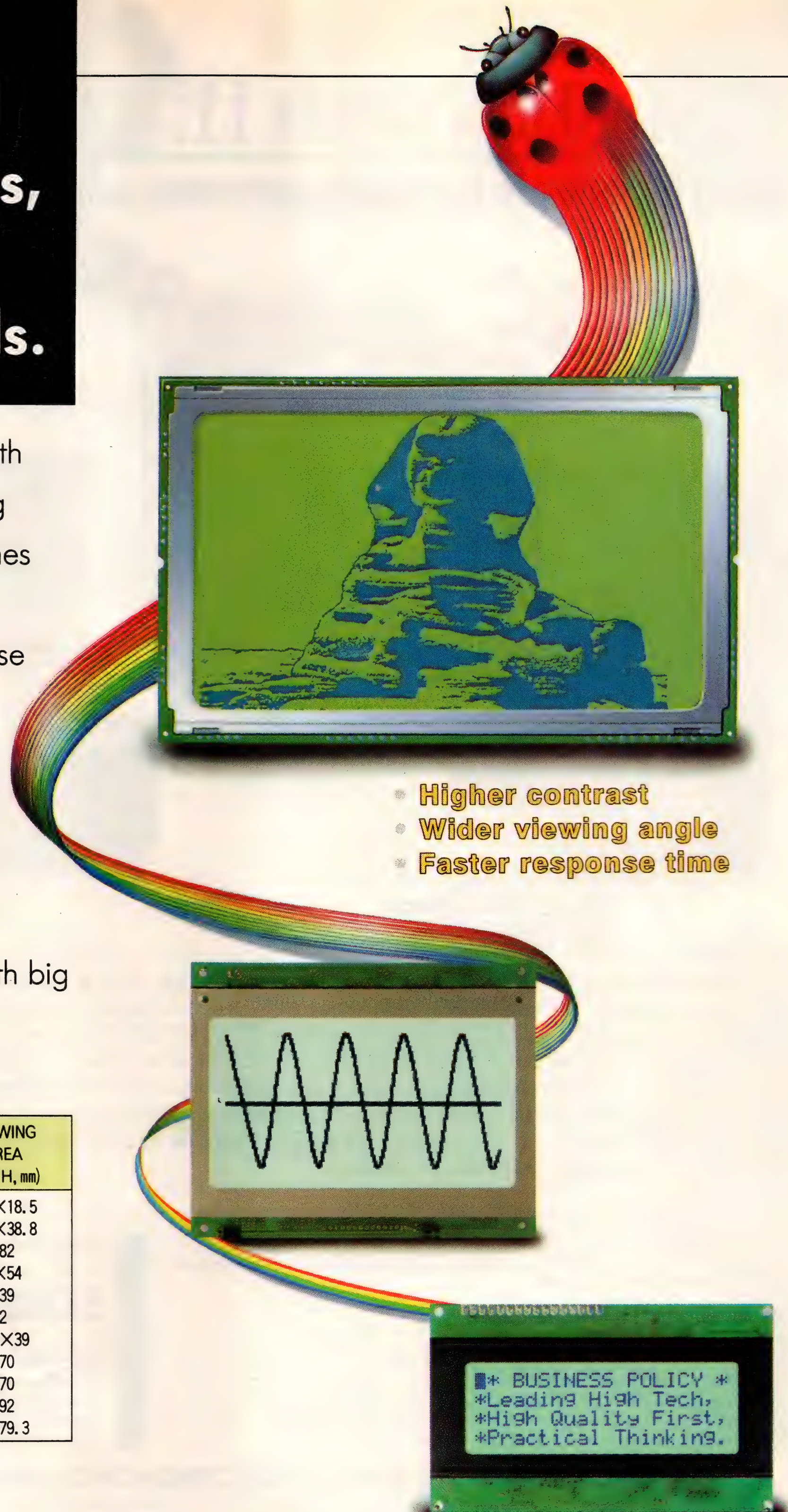

■ STN GRAPHIC TYPE

ITEM / MODEL	DOT NUMBER (W×H, Dot)	EXTERNAL DIMENSION (W×H×D, mm)	VIEWING AREA (W×H, mm)
HG12601	122×32	84×44×16	60.5×18.5
HG12602	128×64	93×70×10	70.7×38.8
HG16501	160×128	129×102×11.5	101×82
HG19501	192×128	98×86×13	77.5×54
HG24501	240×64	180×65×11	132×39
HG24502	240×64	129×62×10	87×42
HG24503	240×64	180×65×10	132.6×39
HG25501	256×128	147×116×12	127×70
HG25601	256×128	147×116×12	127×70
HG32601	320×240	157×110×8.5	121×92
HG32602	320×240	143×96.8×9.5	104×79.3

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CIRCLE NO. 205

Complies with IEC Standard 555-2

When it comes to harmonic currents measurement, leave it to KIKUSUI !

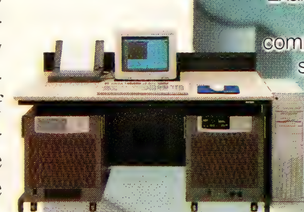
AC power supplies

Windows

PCR-L SERIES

SD02-PCR-L (Application with Linzo)

Measurement of harmonic currents typically requires a multiple number of instruments, including an AC power supply, current sensor and power analyzer. The result is considerable time and trouble. The measurement method offered by KIKUSUI could not be any simpler. Simply connect*1 a personal computer installed with the SD02-PCR-L "Applications with Linzo" harmonic currents analysis program to a member of the PCR-L series of high-performance AC power supplies equiped with a built-in harmonics measuerment function (FFT analyzer). No other instruments are required. Even beginners will be able to measure harmonic currents*2 based on the prosed revision of IEC555-2 while taking advantage of the easy operating environment provided by Windows.*4



Example of a measurement system that combines an AC power supply (PCR2000L) with the optional line impedance network*3 (LIN40M-PCR-L) sold separately.

Notes:

*1 A GPIB cable and optional GPIB interface (Model IB11-PCR-L) sold separately are required for connecting a member of the PCR-L series to a personal computer.

*2 Instruments for fluctuating harmonic currents measurement and flicker measurment are under development.

*3 The Line Impedance Network (model LIN40M-PCR-L) can only be used in combination with the PCR2000L or PCR4000L.

*4 Windows is a trademark of Microsoft Corporation

Intelligent AC Power Supply

PCR-L Series *(8 Models)*

- Max. output capacity: 1ϕ 500 VA to 18 kVA
- Output voltage: 1 to 300 V (switched between 100 V or 200 V range)
- Max. output current: 2.5 A to 90 A (at 200 V range)
- Output frequency: 1 to 999.9 Hz

Harmonic Currents Analysis Program

(Exclusively for use with members of the PCR-L series)

SD02-PCR-L *(Program Name: Applications with Linzo)*

- Operating OS: Windows 3.1/ package: 3.5" floppy disc
- Accommodates harmonic currents measurement based on the proposed revision of IEC555-2.
- Enables harmonics spectrum display, current waveform display, peak current measurment, apparent power measurement and power factor measurement, etc.

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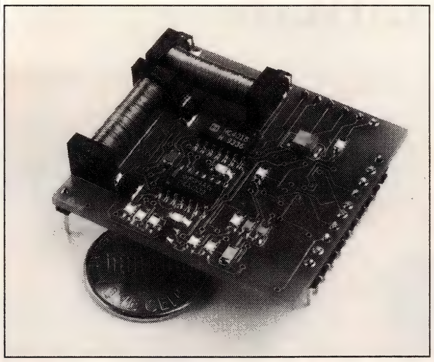
POLAND	ELSINCO POLSKA SP .Z.O.O.	TEL (22) 39 69 79

CIRCLE NO. 92

$6995. **Texas Microsystems Inc**, Houston, TX. (713) 541-8200.
Circle No. 483



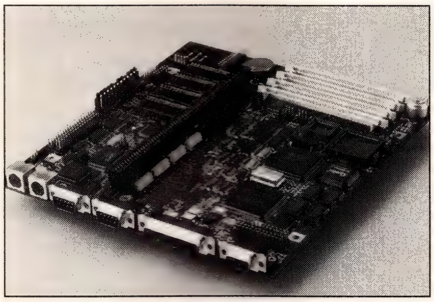
Electronic compass module costs $50. The Vector-2X compass module provides 2° accuracy and 1° resolution in a matchbox-sized module. Using a proprietary magneto-inductive technology, the device draws <10 mA at 5V and <1 mA in power-down mode. The module transmits data in a three-wire serial format that is pin-selectable to be BCD or binary. The two-axis magnetometer has no moving parts. **Precision Navigation Inc**, Mountain View, CA. (415) 962-8777. **Circle No. 484**

Development kit for Access.bus applications. The Access.abl development kit is for developers using the Microchip Technology PIC microcontrollers for Access.bus applications. The kit demonstrates the use of the PIC16C64 and PIC16C74 in applications and provides an ISA bus card, a project card, and software for developing new Access.bus systems. The kit also supports the system-management bus, which Intel and Duracell developed for battery-system management. $495. **Momentum Microsystems Inc**, Colorado Springs, CO. (719) 540-8338.
Circle No. 485

Evaluation board for speech-compression algorithm. The Q0810 PC plug-in vocoder evaluation board lets you evaluate the performance of the Q4400 single-chip variable-rate vocoder. The algorithm compresses digitized speech to bit rates from 2 to 9.6 kbps. The board lets you compare the speech quality of various compression rates with uncompressed speech. The board costs $1595. **Qualcomm Inc**, San Diego, CA. (619) 587-1121.
Circle No. 486

External video-audio unit includes 181-channel, cable-ready TV tuner. The PC/TV provides 24-bit color, fully scalable, full-motion video. The unit supports VGA, SVGA, and XGA at resolutions exceeding 1280×1024 pixels in noninterlaced mode. The external unit does not drain CPU resources, interfere with PC applications, or require an expansion slot. $455. **Rexon Inc**, Simi Valley, CA. (805) 583-5255.
Circle No. 487

Royalty-free ROM BIOS for 80386-EX processor. The BIOS/EX supports 386-EX hardware devices. The kit includes >45,000 lines of assembly-language source code, ROM-disk-generation tools, and the binary configuration program for $4500. The BIOS also requires a $995 CPU personality module. **General Software**, Redmond, WA. (206) 391-4285. **Circle No. 488**



AT-compatible single-board computer suits embedded-control applications. The AT-compatible PrimePlus single-board computer comes in an 8×9-in. form factor. In addition to standard-processor and I/O functions, the board has a ROM disk, SVGA graphics for driving CRTs and LCDs, key-switch scanning, a watchdog timer, two RS-232C/422/485 ports, power management, and expansion capability for both standard ISA cards and the company's miniature expansion modules. The board costs $571 (100). **Dovatron International Inc**, Longmont, CO. (303) 772-5933.
Circle No. 489

Real-time operating system for Motorola's PowerPC single-board computer. The LynxOS for PowerPC 60X comes as a team-development system for the MVME1603 single-board computer. The system includes a 10-user license for AIX-hosted cross-development, the operating system, the

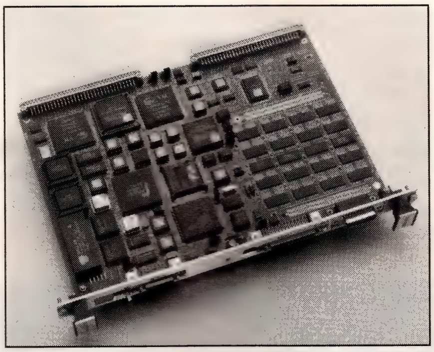
Transmission Control Protocol/Internet Protocol, and the Network File System server and client. The $25,000 price includes a license to run the operating system on one target. **Lynx Real-Time Systems Inc**, Los Gatos, CA. (408) 354-7770. **Circle No. 490**

Embedded PC in 4.5×4.9-in. form factor runs Windows and QNX. The 5025A comes with either a 386CX or a 486SLC operating at up to 50 MHz. The board has three solid-state disk drives that can be custom-configured. One disk contains the AT-compatible BIOS with industrial extensions and DOS 6.0 in 512 kbytes of ROM. You can install QNX or other real-time operating systems in place of DOS. The second solid-state disk stores the application program and can have either 1 Mbyte of EPROM or 512 kbytes of flash memory. The third disk can have 512 kbytes of SRAM, 512 kbytes of flash, or 1 Mbyte of EPROM. The board operates from –40 to +85°C. Prices start at $250 (OEM). **Octagon Systems**, Westminster, CO. (303) 430-1500. **Circle No. 491**

Passive-backplane single-board computer for PCI/ISA. The PCI-930, a 486DX-based CPU card, complies with Revision 2.0 of the Peripheral Component Interconnect (PCI) specification from the PCI Industrial Computer Manufacturers Group. The device is compatible with PCI and ISA bus passive backplanes. The board includes hard- and floppy-disk controllers and serial, parallel, and keyboard ports. It can have as much as 128 Mbytes of DRAM and 4 Mbytes of flash memory. Processor options range from a 50-MHz 486DX2 ($1595) to a 100-MHz 486DX4. **Teknor Microsystems Inc**, Boisbriand, PQ, Canada. (514) 437-5682. **Circle No. 492**

VME board offers PC/AT-compatible computer. The 6U XVME-675 VMEbus board includes a 100-MHz 80486DX4 processor and 16 or 32 Mbytes of dual-access DRAM. The board operates as a 32-bit VMEbus master and provides a slave interface and a PC/104 expansion site. An onboard SVGA controller supports resolutions up to 1024×768 pixels with 256 colors. Other features include two RS-232C ports, a Centronics parallel port, floppy-disk and IDE hard-disk controllers, and a PS/2-compatible keyboard and mouse port. From $5300. **Xycom**, Saline, MI. (313) 429-4971. **Circle No. 493**

Video-graphics accelerator provides 1280×1024 digital video playback at 30 frames/sec. When populated with 4 Mbytes of VRAM, the Viper Pro Video provides 24-bit true color at 1280×1024 resolution and 16-bit color at 1600×1200 resolution. The board costs $679. An upgradable, 2-Mbyte version provides 24-bit color at 800×600 resolution and costs $479. **Diamond Multimedia Systems Inc**, Sunnyvale, CA. (408) 736-2000. **Circle No. 494**



VMEbus CPU board has MIPS R3081E RISC processor. The Malibu CPU board is intended for compute- and I/O-intensive applications, such as video-on-demand, simulation, machine vision, communications, and high-speed printing. The board features 32 Mbytes of two-way interleaved DRAM, Ethernet, SCSI, and a master/slave VSB interface. The board costs $4995 with 8Mbytes of DRAM. **Heurikon Corp**, Madison, WI. (608) 831-5500. **Circle No. 495**

Universal development system provides full-speed real-time emulation for PIC16C5X microcontrollers. The PICmaster-16D Universal In-Circuit Emulator System operates at 20 MHz and runs under Windows. The system includes an emulator-control pod, target-specific emulator Probe-16D, Pro Mate programmer, PC-host-interface card, PC-host-emulation-control software, demonstration hardware and software, and complete documentation. Current PICmaster-16A owners can upgrade for $250. The full system costs $3750. **Microchip Technology Inc**, Chandler, AZ. (602) 786-7200. **Circle No. 496**

PC-based frame grabber provides 8-bit gray scale depth at 512×512 resolution. The M-Vision 200 is a half-slot ISA-bus card that captures video from any RS-170 or CCIR video source in $^1/_{30}$ second. A low-resolution 256×256-pixel mode captures video in $^1/_{60}$ second for situations where object motion is a problem. Image-capture results are stored in onboard, memory-mapped VRAM, buffering the vision system from delays inherent in ISA bus data transfers. $495. **Mu Tech Corp**, Woburn, MA. (617) 935-1770.

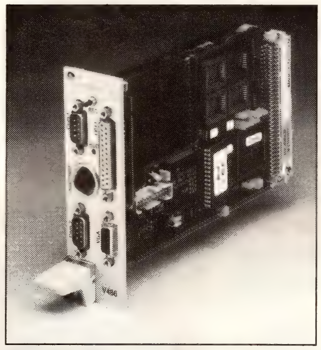
Circle No. 497

VME boards sample dual analog channels at up to 2 MHz. The DVME-614F1 ($2850) samples each channel at 2 MHz with 12-bit resolution. The DVME-614G1 ($3050) samples each channel at 1 MHz with 14-bit resolution. Both boards have FIFOs that let you stream data to disk without interrupting the conversion process. **Datel Inc**, Mansfield, MA. (508) 339-3000.

Circle No. 498

Demo board for evaluating gm833x2 image-resizing chip. The PC-833x2 demo board lets you implement and evaluate the company's image-resizing technology. The package includes schematics, software, and hardware. Dual on-chip DSPs provide up to 33-tap vertical and horizontal FIR filters for image resizing, cropping, panning, and arbitrary positioning of the resize windows in the input and output frame buffer. The system is compatible with Y/C, composite, NTSC, and PAL input and output signals. The demo board costs $3995, and the design kit, without the board, costs $995. **Genesis Microchip Corp**, Mountain View, CA. (415) 428-4277.

Circle No. 499

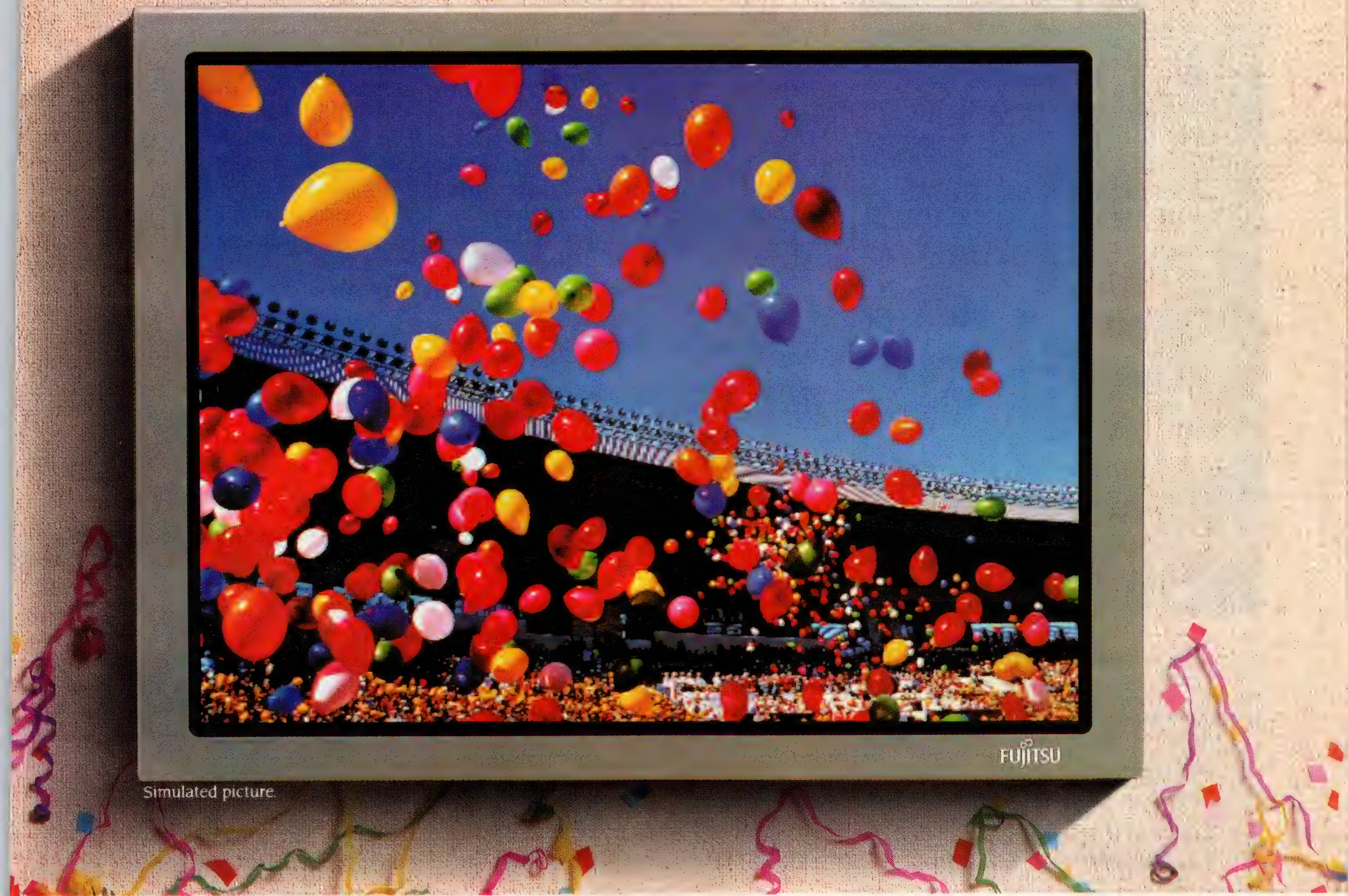


3U VME board has 80486 processor for embedded-PC applications. The V486 uses a 486SX, DX, or DX2 processor and provides all the functions of a PC motherboard, including super VGA graphics, floppy- and hard-disk interfaces, keyboard and mouse interfaces, one parallel and two serial ports, and up to 32 Mbytes of DRAM. The board requires two 3U VME slots and has an ISA bus interface through a special connector for connecting PC-mezzanine boards. The mezzanine connector accommodates stacks of up to three mezzanine boards. With a 486DX2-66 and 4Mbytes of DRAM, the board costs $4650. **PEP Modular Computers**, Scottsdale, AZ. (602) 483-7100.

Circle No. 500

PCMCIA audio cards provide 16-bit resolution. The PCMCIA 16-bit Audio Adapter ($150) supports

Kicking off the color plasma display age!



Slim, light-weight design allows for on-the-wall installation. 260,000-color plasma display from Fujitsu. Now on sale worldwide.

Over the years, Fujitsu has applied leading-edge technology in its commitment to improve plasma displays. This experience and constant effort have paid off — Fujitsu proudly introduces the color plasma display! These displays will revolutionize color presentation, which has been limited to CRT monitors until now. They can be used in a variety of situations, as a new communication tool that can display text and image-based information wherever large numbers of people gather — offices, transportation centers, retail outlets, and financial organizations, to name a few.

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- Slim (32 mm), light-weight (4.8 kg, 10.7 lbs) design allows for on-the-wall installation.
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- High visibility due to a brightness of 180 cd/m^2 (at typical) and a viewing angle of more than 140 degrees.
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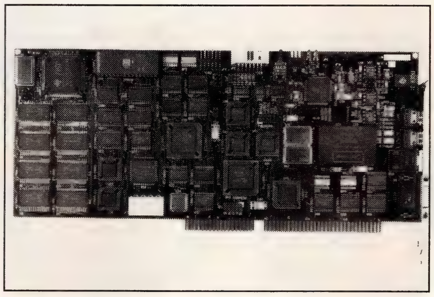
CIRCLE NO. 87

OS/2 and Windows applications and some DOS applications. The card supports Wavetable MIDI synthesis and Microsoft's Sound System 2.0. The PCMCIA Advanced Audio Adapter ($285) supports Windows and DOS applications, including applications designed to use Sound Blaster and Wavetable MIDI. **IBM Microelectronics**, Hopewell Junction, NY. (800) 426-0181. **Circle No. 501**



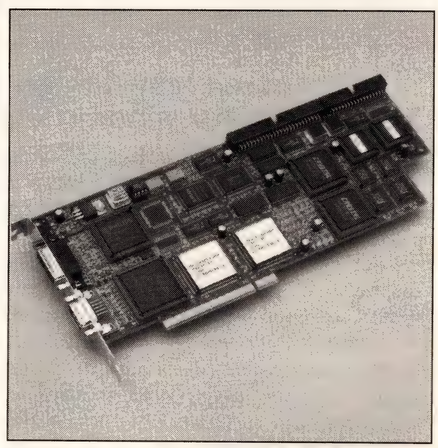
TMS320C31 ISA-bus board for coprocessing or stand-alone operation. The Tiger31/PC runs at 60 MHz and is intended for multimedia-application development, such as modem, fax, telephony, speech, and high-quality audio. The board accommodates up to 1 Mbyte of zero-wait-state SRAM. Two input and output channels offer 16-bit, 50-kHz CD-quality analog. For fax and modem applications, the board has a built-in standard analog telephone interface, FCC part 68 approved. From $2995. A low-cost version is available for OEM applications. **DSP Research**, Sunnyvale, CA. (408) 773-1042. **Circle No. 502**

Single-board computer for VMEbus uses 68060 microprocessor. The SYS68K/CPU-64 has a VME64-compliant VMEbus interface. The device offers 32 Mbytes of shared DRAM, a DMA controller, and SCSI-II and Ethernet interfaces. The 6U VME board costs $5500 for the 50-MHz version. **Force Computers Inc**, San Jose, CA. (408) 369-6000. **Circle No. 503**

Catalog of VMEbus boards for embedded-PC and industrial computer systems. The 140-pg free catalog covers the company's CPU, I/O, and expansion boards. **Arcom Control Systems Ltd**, Cambridge. (44) (0) 223 411200. **Circle No. 504**

Emulation for Motorola microcontrollers offers full-speed operation. The HP64700 system provides emulation for the 68331, 68332, 68F333, and 68336 microcontrollers. Dual-ported emulation memory lets you modify and display many C and assembly-debug functions, such as setting breakpoints and editing C variables, without interrupting program execution. The HP64700B card cage costs $7650; the HP64704 80-channel emulation bus analyzer module costs $3615; and the HP64748C emulation control card costs $5630. Active probe emulators for the microcontrollers cost $4000 each. **Hewlett-Packard**, Santa Clara, CA. (800) 447-3282. **Circle No. 505**

PC/104 CPU module uses the Cyrix 486SLC2. The CoreModule/486-II includes two serial ports, a bidirectional parallel port, keyboard and speaker interfaces, a bootable solid-state disk, and up to 16 Mbytes of DRAM. The 3.6×3.8-in. card dissipates 3W active and starts at $359 (1000) with zero RAM. **Ampro Computers Inc**, Sunnyvale, CA. (408) 522-2100. **Circle No. 506**



Real-time, full-motion JPEG compression and playback PCI board. The Imascan/JPEG board is compatible with CCIR 601 video I/O (720×486-pixel NTSC, 720×576 pixel-PAL) and has four channels of 16-bit audio, bit-rate control, using the Zoran JPEG codec and PCI bus-mastering. $2495. **Imagraph Corp**, Chelmsford, MA. (508) 256-4624. **Circle No. 507**

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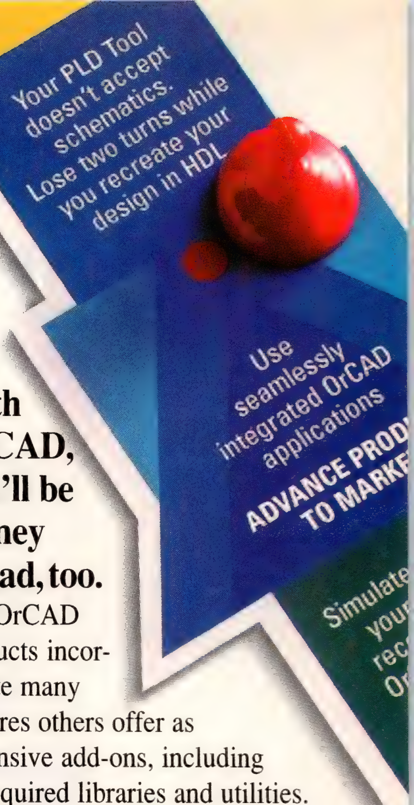

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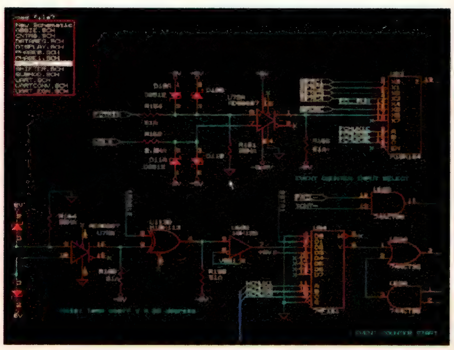

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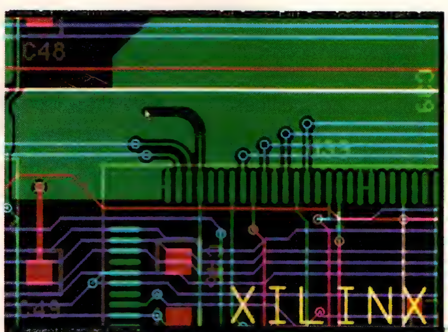

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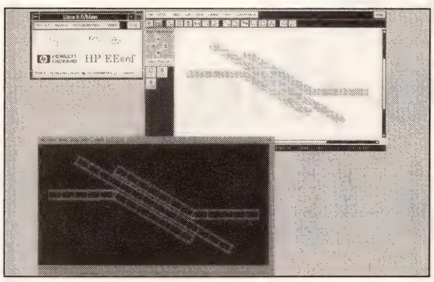
Graphical programming tool automatically generates ST62 μC programs. The ST62-Realizer runs under Windows and lets you create graphical schematic designs of systems from a library of symbols. When you complete the system design, the software automatically generates assembly-language program code for the ST62 family of μCs. The software provides a virtual test bench for use in analyzing and debugging the design. $395. **SGS-Thomson Microelectronics**, Lincoln, MA. (617) 259-0300. **Circle No. 464**

Bidirectional translator for OrCAD and other popular pc-board CAD systems. The bidirectional translator for OrCAD's PCB 386+ system works with 21 other pc-board CAD formats. The translators cost $995 for a 16-bit DOS version, $1495 for a 32-bit DOS version, and $1995 for Sun- and HP-Unix versions. **Router Solutions Inc**, Newport Beach, CA. (714) 721-1017. **Circle No. 465**



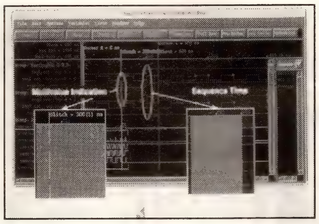
Planar electromagnetic simulator expands the range and accuracy of passive-circuit libraries. Release 2.0 of HP Momentum, available in May, works with high-frequency circuit simulators or as a stand-alone tool to compute S, Y, and Z parameters of general planar circuits. Circuit topologies include micro-strip, strip-line, slot-line, and coplanar waveguide. Some new features include adaptive-frequency sampling, which more accurately models details when S parameters are changing rapidly; edge mesh, which automatically places a row of cells along the edge of the pattern; and far-field plots, which analyze radiating structures, such as patch antennae. The tool comes integrated with the company's Series IV high-frequency CAE-design suite and costs $24,000. **HP-EEsof**, Westlake Village, CA. (818) 879-6200. **Circle No. 466**

Software generates fuzzy-logic systems from user-supplied data. Rule Maker, an add-on to the company's CubiCalc line of fuzzy-logic development tools, automatically generates fuzzy sets. The tool is particularly useful for helping new users develop a rule base and fuzzy sets. Once the working model is in place, users can tune the system in a variety of ways. The tool combines statistical, analytic, and heuristic methods to develop fuzzy-logic systems, even when data is sparse. The tool can create systems with up to nine input variables and three output variables. $195 in North America. **HyperLogic Corp**, Escondido, CA. (619) 746-2765. **Circle No. 467**

Software provides IBM 5080 graphics terminal. The GSE5080 software, running on an HP workstation, lets you view and edit mainframe CAD/CAM/CAE drawings or models while simultaneously running other applications in a multiwindow environment. $2500. **Spectragraphics Corp**, San Diego, CA. (619) 450-0611. **Circle No. 468**

Component library for VHDL provides over 3000 devices. The Standard Component VHDL Library (SCVL) provides high-level VHDL models in a variety of standard parts and memories. The models provide advanced features, such as timing back-annotation and load-dependent delay calculations. The library costs $995 for PCs and $2995 for workstations. **Computer Aided Software Technology Inc**, Pomona, NY. (914) 354-4945. **Circle No. 469**

Waveform viewing and analysis tool provides new capabilities. Signalscan Pro lets you visualize the behavior of a design being simulated from multiple interactive views, including a source-code view. A



feature, called Sequence Time, lets you expand the time steps to view the sequence of events graphically within each time step. The tool provides different views of a design, including source code, waveform, or register views, to help speed debugging. The product lets you invoke and control your Verilog simulator from within the tools' environment. The software starts at $3995. Signalscan 4.0 has many of the capabilities of Signalscan Pro and starts at $2995. **Design Acceleration Inc**, San Jose, CA. (408) 559-8500. **Circle No. 470**

Fault simulator provides new timing capabilities. The TDX-FSIM V3.2 concurrent fault simulator grades test vectors on state and timing sensitive circuits, including synchronous and asynchronous designs. The tool now has pin-to-pin timing capability that simplifies modeling by letting you specify timing at macro boundaries. It also accommodates Standard Delay Format (SDF) timing data and translates Zycad fault lists into TDX format. $9995. **Attest Software Inc**, Santa Clara, CA. (408) 982-0244. **Circle No. 471**

PC X server software lets you run Mentor Graphics applications. XoftWare/32 for Windows, EDA Edition, and XoftWare/32 for Windows NT, EDA Edition, lets you run Mentor Graphics applications, including Design Architect and Design Manager on virtually any Unix system. The products include customized features, such as complex cursor support, expanded font, and predefined start-up icons. Either package costs $495 for a single-user license. **Age Logic Inc**, San Diego, CA. (619) 455-8600. **Circle No. 472**

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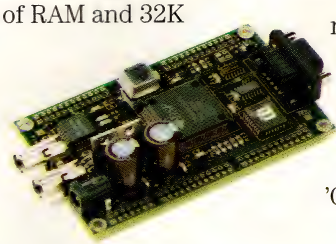

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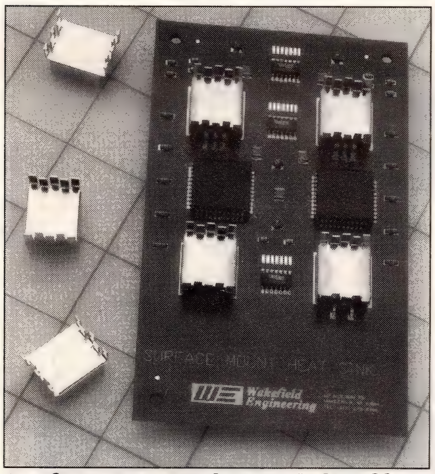


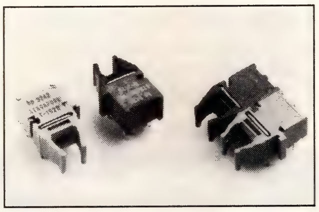
Surface-mount heat sink offers higher power dissipation. The 216 Series surface-mount heat sink measures 0.740 in. wide×0.60 in. long ×0.40 in. high and solders directly to a pc board. Devices generate heat that is conducted through the pc board and dissipated through the heat sink into ambient air. The copper heat sinks with tin-plated leads cost $0.14 (1000). **Wakefield Engineering Inc**, Wakefield, MA. (617) 245-5900. **Circle No. 438**

Illuminated pushbuttons and indicators accommodate snap-in-panel or pc-board mounting. The Cutler-Hammer Series 200 line of illuminated pushbuttons and indicators is rated for 5A at 250V ac. Fingertip-removable switch caps and built-in lamp extractors allow you to replace incandescent lamps from the front panel. Other features include LED or incandescent illumination, full or split legend caps, various colors, and gold contacts for low-level switching. $3 to $8 (100). **Eaton Corp, Aerospace and Commercial Controls**, Milwaukee, WI. (414) 449-7483. **Circle No. 439**

Metalized-polyester film capacitors provide Class X2 interference suppression. Type 924X capacitors suit use in line-bypass, antenna-coupling, across-the-line, and spark-killer circuits and to EMI-filter and switching-power-supply applications. Capacitance ranges from 0.001 to 0.47 μF. Voltage rating is 250V ac. From $0.15 (1000). **Tecate Industries Inc**, El Cajon, CA. (619) 448-4811 **Circle No. 440**

Automotive relays accommodate high currents in small space. The CF relays measure 22.5×16.5×16.5 mm and handle a 10A continuous current and 30A inrush currents. Operating-temperature specifications are –40 to +85°C. The relays have high shock and vibration resistance and are rated for 200,000 operations at the rated load. $2.30 (1000). **Aromat Corp**, New Providence, NJ. (908) 464-3550. **Circle No. 441**

Two-piece PCMCIA card kit uses ultrasonic welding. The US series housings for Type I and II PCMCIA cards snap together and then ultrasonically weld in <1 sec. The series is designed for 88-pin DRAM cards; 68-pin memory cards; and 9-, 15-, 25-, and 32-position I/O cards. The housings are available with and without a label recess. $2.72 (1000). **Hirose Electric Inc**, Simi Valley, CA. (805) 522-7958. **Circle No. 442**



10-Mbps fiber-optic link works with 1-mm plastic and HCS fiber. The HFBR-0508 comprises the HFBR-1528 transmitter and the HFBR-2528 receiver. The transmitter and receiver suit industrial applications, such as machine and robot control. The devices can be 50m apart with plastic optical fiber or 500m apart with hard-clad-silica (HCS) fiber. The HFBR-1528 costs $6.35 (500), and the HFBR-2528 costs $11.10 (500). **Hewlett-Packard Co**, Santa Clara, CA. (800) 537-7715, ext 8958. **Circle No. 443**

90° LED holder works individually or in arrays with T-1¾ or rectangular LEDs. The 922 and 923 Series LED holders mount LEDs horizontally in single- or two-tiered vertical stations. The holders are molded from black nylon. Typical pricing is $77.50/1000 (10,000). **Bivar Inc**, Irvine, CA. (714) 951-8808. **Circle No. 444**

Ceramic resonator provides simple, low-cost microcontroller clock. The ZTS ceramic resonator with a built-in capacitor provides a ±0.3% frequency tolerance and costs $0.18 (10,000). The resonators have a 2- to 12-MHz frequency range and operate down to 1.85V. **Integrity Technology Corp**, Santa Clara, CA. (408) 262-8640. **Circle No. 445**

Dual-winding transformers suit surface-mount applications. The POWER-PAC series of toroidal transformers comes in inductance ranges of 10 to 300 μH and current ratings to 4A. The transformers provide 500V-ac winding-to-winding isolation and easy solder-joint inspection. Typical price is $2 (10,000). **GFS Manufacturing Inc**, Dover, NH. (603) 742-4375. **Circle No. 446**

Fiber-optic receiver for 16-Mbps token-ring applications. The HFM1220 receiver meets IEEE 802.5J

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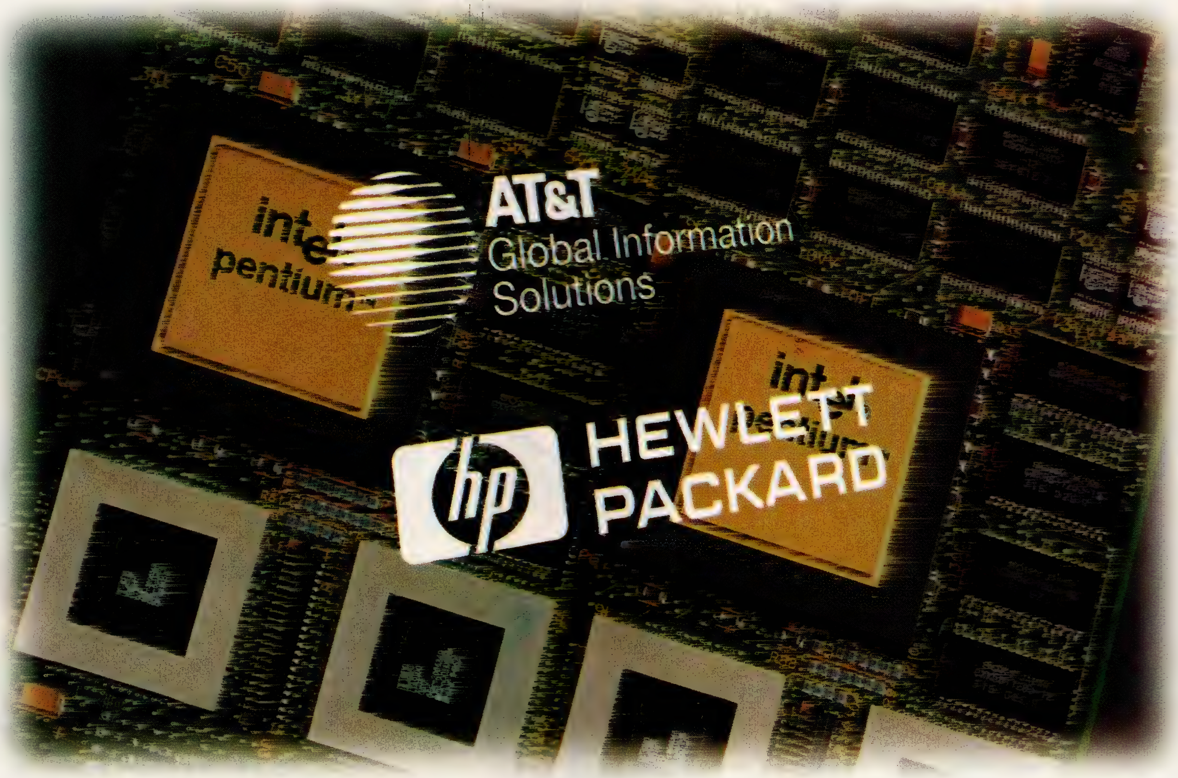

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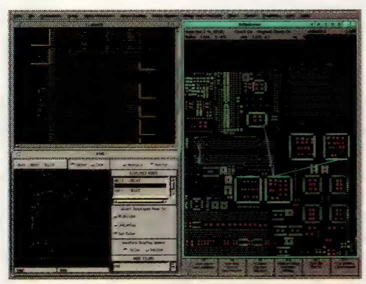

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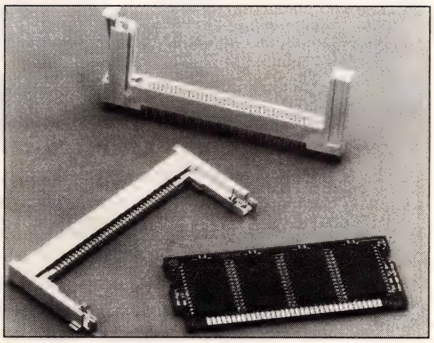
signal standards. A PIN photodiode and a preamp are mounted in the fiber-optic connector for current-to-voltage conversion. The device has a 500Ω output-drive capability and –31- to –11-dBm sensitivity. The 16-pin DIP module costs $21.95 (1000). **Micro Switch**, Freeport, IL. (800) 367-6786. **Circle No. 447**

Heat sinks suit 90- and 100-MHz Pentium processors. The Penguin Coolers 798-pin-fin heat sinks provide fin-to-channel ratios in the range of 10:1 for a large effective heat-dissipation surface area. The 2.1×1.92-in. heat sinks are available in heights from 0.4 to 1 in. For the lowest cost adhesive assembly, the heat sinks are available with preapplied, pressure-sensitive, acrylic adhesives. From $1.37 (1000). **Wakefield Engineering Inc**, Wakefield, MA. (617) 245-5900. **Circle No. 448**



DIMM socket provides efficient use of pc-board space. The M3 small-outline, dual-in-line, memory-module (SO-DIMM) socket requires half the board space of a standard SIMM socket. The 72- and 88-position SO-DIMMs cost $0.03 to $0.05 per line (10,000). **Amp Inc**, Harrisburg, PA. (717) 564-0100. **Circle No. 449**

50W power MOSFET provides circuit-breaker-type action for overload and overtemperature conditions. The HAF2001 is a 10A silicon N-channel device that is fully tolerant of short circuits. Under conditions where traditional power transistors would fail or burn, the device turns off and remains off until reset by connecting the gate terminal to ground. The device provides adjustable rise time to reduce EMI. $1.55 (1000). **Hitachi America Ltd, Semiconductor & IC Division**, Brisbane, CA. (800) 285-1601, ext 90. **Circle No. 450**

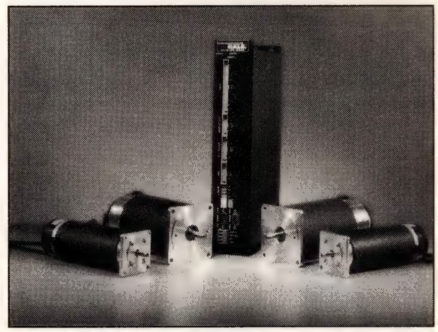
Network enclosure for PC servers. The Server cabinet is a universal cabinet frame with recessed mounting. The cabinet accommodates desktop, tower, or rack-mount servers, monitors, and keyboards; UPS systems; and other networking components. The basic unit consists of an aluminum frame, removable steel-side panels and rear door, a Plexiglas front door, and an integral cooling system. Optional accessories include stationary or telescopic shelves, casters or adjustable feet, and 19-in. rack-mounting rails. From $1475. **Schroff Inc**, Warwick, RI. (401) 732-3770. **Circle No. 451**

Dual-surface-mount NPN transistor pair is QPL approved in accordance with MIL-S-19500/495. The JANTX2N5794U and JANTXV25794U

transistor pairs are hermetically sealed in a ceramic LCC six-pin package. The transistors are similar to 2N2222. From $15.48 (1000). **Optek Technology Inc**, Carrollton, TX. (214) 323-2200.
Circle No. 452

High-ratio transformer for sensitive current-monitoring applications. The CSE187-L transformer has a 1:500 primary to secondary turn ratio for changing a high current into a low current. The transformer accepts inputs from 0.1 to 30A and provides a typical output of 110 mV/A with a 60Ω load resistor. The 0.7-in.-high transformer is constructed from UL-recognized materials and carries a Class B rating for use in ambient temperature environments up to 130°C. It is designed to withstand a 2500V high pot condition. $1.98 (1000). **MagneTek Inc**, Goodland, IN. (219) 297-3111. **Circle No. 453**

Three new packages for surface-mount LEDs. The microLED product line offers packages starting at 3×1.5×1.5 mm. The devices include a highly reflective, white-ceramic substrate that helps direct the light and acts as a heat sink. The devices are available in red, green, and yellow. Bicolor devices are available in larger packages. From $0.26 (1000). **Dialight Corp**, Manasquan, NJ. (908) 223-9400.
Circle No. 454



Stand-alone motion controller offers speed and precision. The DMC-1500 Series stand-alone motion controller provides one to eight axes of control with step motors, servo motors, and hydraulics. The controller uses a 32-bit μP to provide 8 million counts/sec encoder feedback and an 8000-Hz update rate per axis. A 14-bit motor-command output DAC with PID filter has velocity and acceleration feedforward for precise positioning. Programs store nonvolatile EEPROM. Two RS-232C or RS-422 ports provide communication. Prices range from $995 (100) for one axis to $1595 (100) for eight axes. **Galil Motion Control Inc**, Sunnyvale, CA. (408) 746-2300.
Circle No. 455

Low-profile pc-board-mount transformer suits VDE requirements. The SPW-2100 6-VA transformer has outputs from 5 to 230V ac. The 0.9-in.-high transformer is interchangeable with the company's SPW-100 Series. Units are fully immersed in epoxy, permitting aqueous and solvent pc-board cleaning. Approvals are pending for VDE 0805, UL 1950, UL 1585 Class II and III, and IEC 950. $4 in quantity. **Prem Magnetics Inc**, McHenry, IL. (815) 385-2700. **Circle No. 456**

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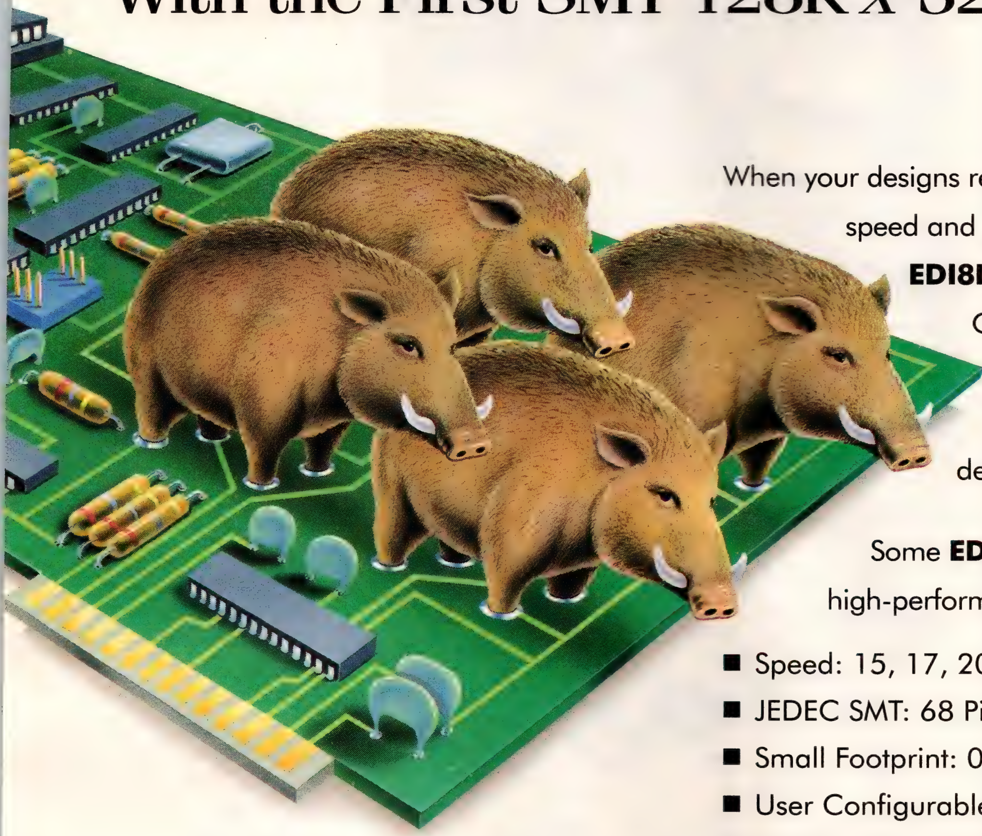

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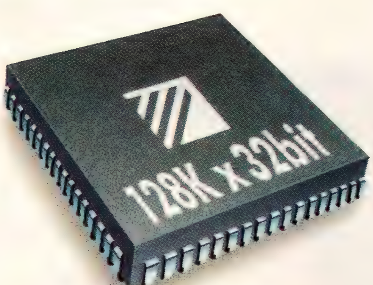

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CIRCLE NO. 77

CIRCLE NO. 28

Chip resistors offer Ω to 20 MV values with tolerances of ±1, ±2, and ±5%. The chip resistors are available in sizes 0603, 0805, 1206, and 1210. Power ratings range from 0.031 to 0.25W. Maximum working voltage ranges from 50 to 200V. From $0.005 in production quantities. **International Components Corp**, Melville, NY. (516) 293-1500. **Circle No. 457**

25-GHz RF discrete silicon transistor for wireless applications. The SIEGET grounded-emitter-transistor family includes the BFP 405, BFP 420, and BFP 450. At 2V, the transistors offer gains of 14 to 22 dB at 1.8 GHz. The devices come in an SOT 343 package and cost $0.91 to $1.31 (1000). **Siemens Components Inc, Integrated Circuits Division**, Cupertino, CA. (408) 777-4500. **Circle No. 461**

Pushbutton switches offer 250,000 cycles at 0.4 VA at 20V. The 400 Series pushbutton switches have a tactile response and audible click when actuated. The SPST switches are available in a push-on/push-off or momentary-on configurations. The switches accommodate 3A at 120V ac or 28V dc and are derated to 10,000 cycles. From $2.30 (1000). **Mors/Asc**, Wakefield, MA. (617) 246-1007. **Circle No. 462**

Snap-in mounting slide switches have splash-resistant housing and 11A rating. The LP Series enclosed miniature slide switches are available in SPST, SPDT, DPST, and DPDT models. All model have positive detent and tactile feedback. Electrical life is 10,000 make-and-break cycles at full load. Dielectric strength is 1000V rms at sea level. From $1.04 (1000). **C&K Components Inc**, Watertown, MA. (617) 926-6400. **Circle No. 458**

Pushbutton switch is sealed for severe-environment applications. The Series 84 pushbutton switch is sealed to IP 65 and NEMA 4 and 13 specifications. The switches have a 400g operating force, 1.5-mm travel, and a 1-million-operation mechanical life. Gold-plated contacts are rated at 42V dc/50 mA with an electrical life of 500,000 operations at 42V/100 mA. Available with or without LED illumination, the basic unit costs $5 (100). **EAO Switch Corp**, Milford, CT. (203) 877-4577. **Circle No. 459**

TFT LCD panels come in 9.4- to 12.1-in. sizes. Five thin-film transistor (TFT) LCD panels provide color display with VGA, SVGA, and XGA resolution. Four models offer 4000 colors, and the 10.4-in. NL6448AC33-11 offers full analog color. Samples cost $2000 to $5000. **NEC Electronics Inc**, Mountain View, CA. (800) 366-9782. **Circle No. 460**

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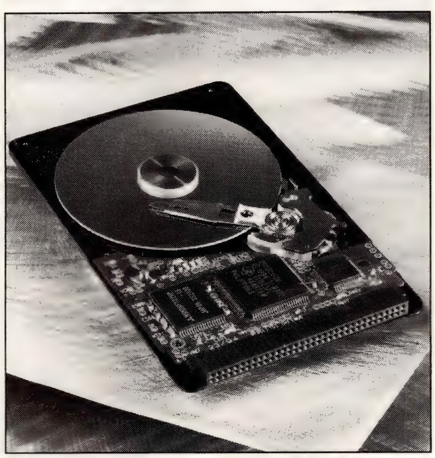
High-accuracy touch screen compensates for CRT image distortion. The ClearTek 2000 analog capacitive touch screen stores a factory touch-screen calibration in nonvolatile memory to provide touch coordinates with less than ±1% offset. The touch screen has an 8- to 15-msec response time and offers 1024×1024 resolution. From $495. **MicroTouch Systems Inc**, Methuen, MA. (508) 659-9000.
Circle No. 510

PCMCIA Type III hard-disk drives offer capacities to 420 Mbytes. The 1.8-in., hard-disk drives challenge 2.5-in. drives on capacity, yet are fully PCMCIA Type III release 2.1 compatible. Shock resistance is 750g nonoperating and 150g operating. Average seek time is 12 msec. The Viper 8260PA has a 260-Mbyte capacity and costs $499. The Viper 8340PA has a 340-Mbyte capacity and costs $599. The Cobalt 8420PA has 420-Mbyte capacity and costs $699. The 8260PA is available now. **Integral Peripherals**, Boulder, CO. (303) 449-8009. **Circle No. 511**



1.8-in. hard drive fits PCMCIA Type II form factor. The MobileMax Lite 85 with 85-Mbyte capacity ($449) and the MobileMax Lite 121 with 121-Mbyte capacity ($499) are only 5 mm thick. The drives feature 3.3V operation and have shock specifications of 1000g non-operating and 180g operating. Spin-up time to transition from a 10-mW sleep mode to an active mode is 1.5 sec. Average seek time is 16 msec. MTBF is 300,000 power-on hours. **Maxtor Corp**, San Jose, CA. (408) 432-1700.
Circle No. 512

17-in. color monitor has 1600×1280 noninterlaced resolution. The 4500DC has a 0.27-mm dot pitch and a 76-Hz refresh rate. Other features include a flat, square screen coated to reduce glare. $759. **Optiquest Inc**, Tarzana, CA. (818) 757-0070.
Circle No. 513

2.5-in. hard drive stores 420 Mbytes in 0.5-in.-high package. The CFL 420A has an average seek time of 12 msec. The device supports the PIO Mode 3 of the Enhanced IDE interface for data-transfer rates of up to 11.1 Mbytes/sec. The drive requires 0.85W in idle mode with the drive spinning but not reading or writing. Power consumption drops to 0.15W in standby mode. The drive weighs 4.9 oz and has an MTBF of 300,000 hours. Shock ratings are 300g nonoperating and 100g operating. $335. **Conner Peripherals Inc**, San Jose, CA. (408) 456-4500.
Circle No. 514

230-Mbyte removable disk drive with five-year warranty. The Bernoulli 230 transportable hard-disk drive uses a removable cartridge. The cartridge can withstand 1000g shocks, minimizing the risk damage if the cartridge is accidentally dropped. The system has a 2.67-Mbyte/sec maximum-transfer rate and an effective access time of 18 msec. Built-in 256-kbyte read/write cache speeds save operations. The MTBF is 200,000 hours. The drive costs $582, and the cartridges cost $119. **Iomega Corp**, Roy, UT. (801) 778-1000. **Circle No. 515**

Symmetric multiprocessor upgrade for 486-based computers. The REV-to-SMP device lets you transform a standard 486-based computer into a dual-processor-based symmetric-multiprocessor (SMP) system by adding a 486SX, a 486DX, a 486DX2, a DX4, or an Intel OverDrive processor. The dual-processor upgrade runs the new generation of operating systems from Banyan, IBM, Microsoft, Novell, SCO, Sun, and others. You can continue to run DOS or Windows applications using OS/2 SMP or Windows NT. The $499 price does not include the proces-

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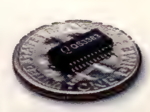

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CIRCLE NO. 110

sors. **Evergreen Technologies Inc**, Corvallis, OR. (503) 757-0934.
Circle No. 516

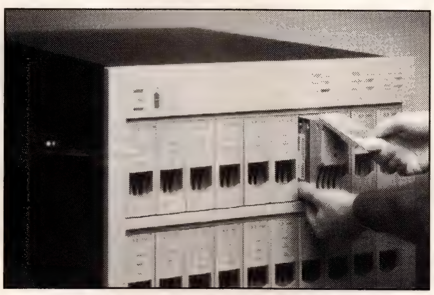
PCMCIA software package diagnoses problems, reduces memory usage, and improves power management. The PCMCIA Power Pack bundle of three products includes CardWizard, CardLite, and CardPower. The CardWizard Windows 3.1 utility assists users in diagnosing and resolving configuration problems. CardLite for the company's CardSoft card-and-socket-services product enables users to balance PCMCIA card support with memory overhead. CardPower, a set of drivers and a user interface, extends power management to PCMCIA slots for increased battery life. The bundle costs $2 to $5 in OEM quantities. **SystemSoft Corp**, Natick, MA. (508) 651-0088. **Circle No. 517**

2- and 4-Gbyte, 3.5-in. hard-disk drives are 1 in. high. The 4.35-Gbyte C3331, 2.17-Gbyte C3330A, and the 2.17-Gbyte C3325A use magnetoresistive heads and partial-response maximum-likelihood (PRML) read-channel technology. The drives provide a 20-Mbyte/sec transfer rate through a SCSI interface. MTBF for the C3325 is 800,000 hours; MTBF is 1,200,000 hours for the others. Prices start at $1775. **Hewlett-Packard Co**, Santa Clara, CA. (800) 826-4111.
Circle No. 518

3.5- and 2.5-in. disk drives offer up to 4.3 and 1.08 Gbytes of storage. The DK328C family of disk drives offers 1 to 4.3 Gbytes in 3.5-in., 1-in.-high drives. The drives transfer data at 11 Mbytes/sec, have a 9.8-msec average access time, and an 800,000-hour MTBF. They cost from $695 to $1935. The 0.75-in.-high, 2.5-in. DK212A drives weigh 200g and store 810 ($850) or 1.08 Mbytes ($995). The 0.5-in.-high, 2.5-in. DK222A drives weigh 135g and store 270 Mbytes ($350) and 540 Mbytes ($595). The 2.5-in. drives transfer data at 11 Mbytes/sec, have a 12-msec average seek time, and a 300,000-hour MTBF. **Hitachi America Ltd, Computer Division**, Brisbane, CA. (415) 589-8300. **Circle No. 519**

System combines rewritable optical storage and quad-speed CD-ROM. The Phasewriter dual 5.25-in., half-height drive uses two types of media: all standard CD formats, including CD-DA; CD-ROM modes 1, 2, XA, and Photo CD; and 650-Mbyte rewritable phase-change optical disk in CD size. The phase-change optical disks are rated for more than 500,000 write cycles. $1000. **Toray Optical Storage Solutions**, San Mateo, CA. (415) 341-7152. **Circle No. 520**

Hard-disk drives provide high capacity in small form factors. The MK-1924 provides 540 Mbytes of storage with a 13-msec average seek time in a 0.5-in.-high, 2.5-in. drive. The drive transfers data at 16.6 Mbytes/sec, consumes an average of 1W from a single 5V supply, and costs $435. Other 2.5-in. hard-disk drives include the 810-Mbyte MK-2628 ($599) and the 1.08-Gbyte MK-2728 ($699). All of the drives have a 300,000-hour MTBF. **Toshiba America Information Systems Inc, Disk Products Division**, Irvine, CA. (714) 457-0777. **Circle No. 521**



RAID-controller boards and subsystems for OEMs. Series 3 RAIDs (redundant array of independent disks) ensure that end users maintain continuous access to data, even in the event of a failed disk drive. The Series 3 SCSI controllers (from $3100) have a throughput of more than 3000 I/O operations/sec and connect up to 35 drives. The Series 3 SCSI Lite controllers (from $1400) fit into a 3.5-in. disk-drive slot and connect up to 30 drives. Com-

plete Series 3 RAID subsystems providing a maximum of 20 drives and 80 Gbytes of storage are available for 19-in. rack mounting. The subsystems start at $18,400. **AT&T Global Information Solutions, NCR Microelectronic Products Division**, Fort Collins, CO. (800) 334-5454. **Circle No. 522**

Compact removable storage system holds 2 to 15 Mbytes. The CompactFlash (CF) storage system weighs 0.5 oz, is the size of a matchbook, performs all PCMCIA-AT-attachment-bus functions, and has an operating shock rating of 2000g. The card is one-fourth the volume of a standard PCMCIA Type II card. An adapter interfaces the card to Type II and Type III PCMCIA slots. The nonvolatile flash-memory cards suit small, portable products, such as digital cameras, cellular phones, pagers, and handheld computers. OEM volume prices range from $75 for the 2-Mbyte capacity to $345 for the 15-Mbyte capacity. **SunDisk Corp**, Santa Clara, CA. (408) 562-0500. **Circle No. 523**

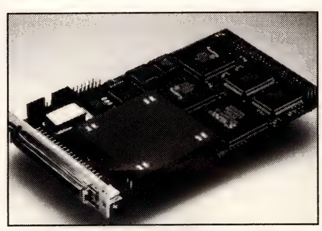
Workstation suits floating-point and cache-memory operations. The SPARCstation 20 model HS11 uses the 100-MHz hyperSPARC processor from Ross Technology and is rated at 104.5 SPECint92 and 127.6 SPECfp92. You can expand the system, which has four SBus slots, to 512 Mbytes of main memory and 2 Gbytes of internal mass storage. The workstation also includes a CD-ROM drive, a 3.5-in. floppy-disk drive, and high-quality audio. It is binary-compatible with existing applications. With 32 Mbytes of main memory, 1 Gbyte of mass storage, and a 17-in. color monitor, the system costs $18,695. **Sun Microsystems Computer Corp**, Mountain View, CA. (800) 821-4643. **Circle No. 524**

Expanded third-party development program suits PowerPC systems. The program includes new reference designs, a reference-design database, availability of reference boards and systems, new hardware and software tools, and a third-party technical-support center. The company sells reference hardware, boards, and systems for third parties to evaluate their development products in a PowerPC system. The boards are for PowerPC 601, 603, and 604 µPs. The average prices for boards and systems are $2500 and $5000, respectively. The reference database, reference designs, modeling, and simulation data are free to qualified third parties. **IBM Microelectronics**, Hopewell Junction, NY. (800) 769-3772. **Circle No. 525**

Alpha-based workstation has PCI bus. The Alpha 64 XP uses a 275-MHz DECchip 21064 Alpha AXP RISC µP with a Peripheral Component Interconnect (PCI) bus for a high-throughput, low-cost, and flexible I/O interface. The workstation has an estimated performance of 130 SPECint92 and 230 SPECfp92. The PC Alpha 64 NT, including 16 Mbytes of memory, a 3.5-in., 1-Gbyte disk drive, a 15-in. color monitor, and Windows NT, costs $12,750. The Alpha 64 XP, including 64 Mbytes of memory, a 3.5-in., 1-Gbyte disk drive, a 15-in. monochrome X-Windows terminal, and OSF/1, costs $22,500. **Aeon Systems Inc**, Albuquerque, NM. (505) 828-9120. **Circle No. 526**

Disk drive provides 100-Mbyte removable storage with 30-msec access time for $200. The 3.5-in. Zip disk drive uses floppy-disk cartridges offering 100-Mbyte ($19.95) and 25-Mbyte ($9.95) storage capacities. The drive is useful as an extension to hard drives and for backup. The average data-transfer rate is 1 Mbyte/sec. **Iomega Corp**, Roy, UT. (801) 778-1000. **Circle No. 527**

Low-cost PCI Ethernet adapter suits twisted-pair networks. The EtherWORKS Turbo Peripheral Component Interconnect (PCI) twisted-pair Ethernet adapter works with PCI-based computers and provides full-duplex, 20-Mbps Ethernet. The network adapter, including driver software, costs $179. **Digital Equipment Corp**, Maynard, MA. **Circle No. 528**



SBus-SCI adapter card lets clustered workstation share memory through 1-Gbps sec link. According to the company, the SBus-scaleable coherent-interface (SCI) adapter card runs four times faster than 266-Mbps Fibre Channel, the next fastest LAN technology currently available. The card has two 1-Gbps links with throughput orders of magnitude faster than Ethernet. Station-to-station latencies are as low as 0.5 µsec. $2650 OEM. **Dolphin Interconnect Solutions Inc**, Westlake Village, CA. (805) 371-9493. **Circle No. 529**

Monochrome monitor has 1024×768-pixel interlaced resolution. The 10-in. ViewMagic Model MD-0935 monochrome monitor has a nonglare screen with a paper-white phosphor. The PC-compatible monitor has a 35W max power consumption reducing to 12W in the standby or suspend mode. The Monitor complies with all major safety regulations, including UL, CSA, TUV/GS, FCC, FTZ, DHHS, and PTB. Suggested list price is $129. **ETC Computer Inc**, Fremont, CA. (510) 226-6250. **Circle No. 530**

SVGA monitor suits small-footprint applications. The 9-in. color monitor has 1024×768-pixel resolution, a 0.28-mm dot pitch, and 65W max power consumption. Safety approvals include low-radiation MPR 11, TUV/GS, FCC Class B, UL, CSA, DHS, and FTZ. Single-unit list price is $529. **Smile International Inc**, Costa Mesa, CA. (714) 546-0336. **Circle No. 531**

Digital-radio modems have –34 to +74°C operating-temperature range. The radio modem contains a UHF radio transceiver that transmits data at 4800 bps. The 0.25W model costs $950 and has a line-of-sight transmission distance of 5 mi. The 1-lb, 7.5×3.6×2-in., 2W radio ($1600) with directional antenna has a tested transmission distance of >20 mi. An intelligent RS-232C communications port provides data-input and -output rates up to 19.2 kbps. **Monicor Electronics Corp**, Fort Lauderdale, FL. (305) 979-1907. **Circle No. 532**

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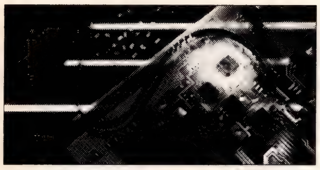

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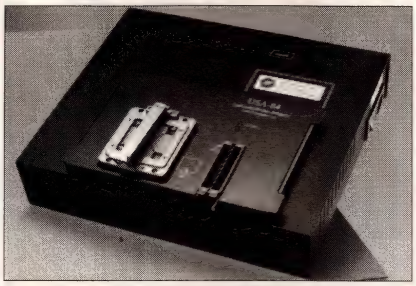

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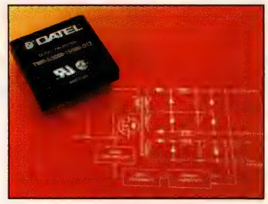

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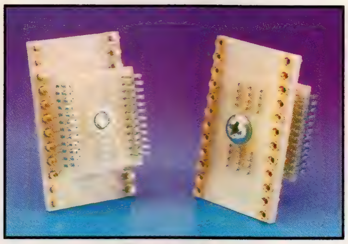

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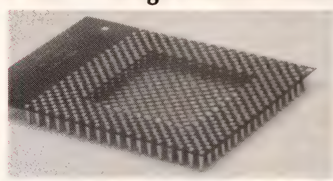

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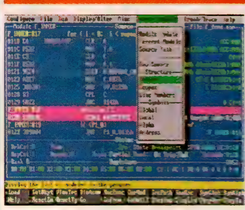

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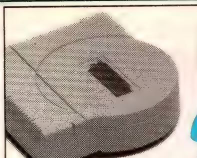

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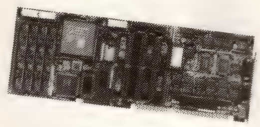

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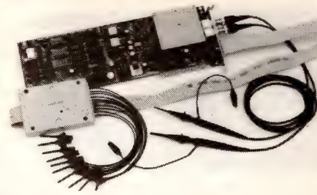

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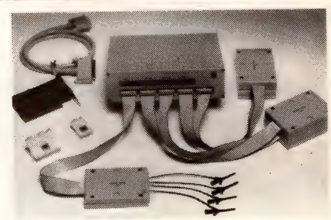

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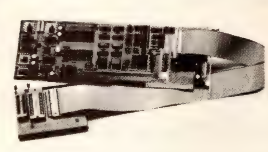

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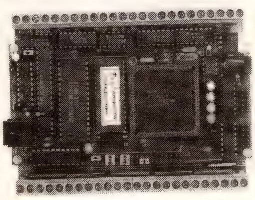

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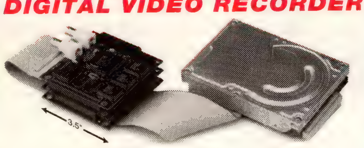

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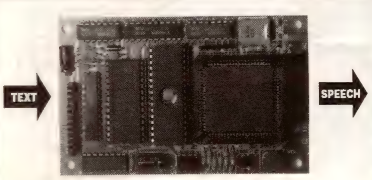

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Design debuggable hardware

A decade ago, Ford Motor Company was bleeding cash. The gas-guzzling American behemoth was rapidly becoming a dinosaur in the wake of an explosion in Japanese auto sales. Something had to be done *fast* for Ford to regain market share and profitability.

In a two-billion-dollar gamble, Ford's engineers designed the Taurus in record time. (Who says big companies are risk-averse?) The new car was revolutionary in many ways, but perhaps the most profound change was a new way to engineer cars. The Taurus project was one of the first major concurrent-engineering designs; that is, everyone having anything to do with the car was involved from the beginning of the design process. From day one, engineering, production, sales, and distribution all worked hand-in-hand to get a quality car to market as quickly as possible.

Don't assume that the software crowd will "come up with something." Because, if it doesn't, your clever design could bankrupt the company.

Now it's fairly common to flip through the pages of a design magazine and see at least a handful of references to concurrent engineering. The old model, where each department worked in isolation before hurling the project to the next group, is quietly fading away. It's impossible to forget the problems that production or sales face when representatives of these groups are staring over the designer's shoulders.

For example, now most every car generates a serial diagnostic stream from the system's master computer. Cars are simply too complex for the average mechanic (let alone most of us part-timers); these error codes use a very slow bit stream specifically tailored to the crummy equipment you'd expect to find in a repair shop. Hook up that slow VOM to ground and the test point and the computer deflect the meter five times for code 5, followed by a pause, then three times for a 3. Look up the codes in your service manual and voila! You'll know what to replace.

Though the big car companies now seem to be masters of engineering, far too many smaller operations still operate in the Dark Ages. It seems the wall between hardware and software development grows each year: Software engineering becomes ever more specialized, and hardware continues to evolve at its customary dizzying pace.

It's scary how many software groups receive a piece of "functional" prototype hardware from designers delivered with schematics—but nothing else. These schematics are usually incomprehensible to the software folks and are made even more obtuse by frequent use of PLDs and similar functional blocks (with perhaps hundreds of connections) plopped down on the page. These blocks are documentation black holes: every signal goes in, and presumably something comes out. But, without the designer's suite of design tools, even the brightest firmware person rarely makes sense of the design.

Where the hardware group's responsibilities end and firmware's begin makes for an interesting philosophical debate. Should the designers include device drivers? How do they know the logic works without writing some sort of code to check out each peripheral? Why not structure the development plan to make this test code part of the framework of the final software? I feel hardware tends to be so complex now that it's unfair to give "naked iron" to the software people. At the very least, deliver low-level drivers with a well-defined interface.

Talk to your software counterparts. You may be surprised to learn that all too often your cool new product makes debugging the code practically impossible. Poor design decisions may seriously impact the firmware schedule.

Mechanical issues

Smaller, faster, cheaper. Chant these words repeatedly, eyes closed, legs lotussed, spirit uplifted. It's the silicon mantra, and it drives electronics to phenomenal success—while turning industry practitioners' hair prematurely gray.

How are you going to connect debugging tools to that tiny new PCMCIA card you're working on? Don't just assume that the software crowd will "come up with something." Because if it doesn't, your clever design could bankrupt the company.

About a year ago, I visited a company in Canada that was facing exactly this problem. The card's CPU had whisker-thin TQFP leads no tool could grab. Because it wasn't a mainstream part, there were no software debuggers available, and, if there were, the ROM/RAM configuration was too tight to allow the extra code a software monitor

PHOTOGRAPHY / HOWARD DAVIS

needs. Their clever solution was to design the card with a rather large extra connector, a simple 100-pin header, with all CPU lines connected. Though the connector doubled the size of the board, it sat alone, the only component outside of the PCMCIA's form factor. Any tool could plug into it, yielding a complete development environment. When it came time to ship the product, designers used a bandsaw to cut the connector and the board down to size. Of course, without the connector, production versions were properly sized cards.

Have you ever worked on military equipment? The boards are usually crammed tightly together and are often conformal-coated. Far too often, an extender card won't work because the CPU becomes unstable driving the extra-long lines. I wonder how much these accessibility issues drive up the defense budget.

Card cages, military or not, are often a source of trouble. Debugging the hardware is difficult enough: try slipping a scope probe in between boards. It's not unusual to see a card with a dozen wires hastily soldered on, snaked out to where the scope or logic analyzer connect.

This situation is totally unacceptable. Why make life difficult? Either design a robust processor board that works properly on an extender or come up with a mechanical strategy that lets you put the CPU near the end of the cage (with the cage's metal covers removed), so you and the software people can gain the access so essential to high-productivity debugging.

One company I know of can only remove the "wrong" (that is, the circuit) side of the card-cage cover. The solution is to solder the processor socket on the circuit side of the board and then make a pin-swapping jig (using parts from Emulation Technology or EDI), to which the company's smart logic analyzer connects. Using a ROM emulator in a similarly tight situation? Consider the same trick of inverting one or more ROM sockets.

SMT packaging

Back in the good old days, microprocessors were available in only a few package types, such as DIPs, PGAs, or PLCCs. These parts were designed for through-hole pc boards with the expectation that, at least for prototyping, designers would socket the processor. Isolating or removing the part for software development required nothing more than the industry-standard chip puller (a bent paper clip or small screwdriver).

There's no cheap cure for the purely mechanical problem of connecting a tool to those whisker-thin pins, but at least the industry's connector folks (Emulation Technology, EDI, Pomona) sell clips that snap right over the soldered-on processor. The clip translates those SMT leads to a pc board with a PGA or header array your tools can plug into.

Where the hardware group's responsibilities end and firmware's begin makes for an interesting philosophical debate.

Getting to the CPU's core is another problem. The Z80 processor, for instance, comes in many flavors. The 84C013 and 84C015 variants are nothing more than a Z80 core with integrated peripherals, all enclosed in a QFP. The Z180 derivative lives on as the core of the highly integrated Z182, also in a QFP configuration.

Zilog dedicated one or two pins (depending on the chip) to selecting "evaluation" modes. Your system drives these inputs to the default state, which lets the CPU fulfill its karma by operating like a normal processor. An emulator, though, can put the part into one of two evaluation modes.

Mode 2 completely tristates the part. It becomes little more than an anchor to connect the adapter and tool. The emulator must replace both the CPU core and the high integration peripherals. Mode 1 tristates only the core and reverses the directions of certain signals. The clipped-on emulator contains just a core replacement (a Z80 or Z180). The peripherals in the processor on your board respond to commands as if no tool were in use. A number of IC vendors use this approach on near-custom processor families (most of which are based on a standard processor core), because it lets the customer use a standard set of widely available development tools.

What does all this mean to the hardware designer? If you connect these evaluation-mode pins directly to ground or V_{CC} to select the default "normal" mode, no tool will ever be able to overdrive these inputs. The evaluation mode will be inaccessible. Have pity on the software folks and use individual pullups and pulldowns instead.

The new 386EX has a similar requirement. One pin, FLT ("float"), tristates the entire device if asserted low. Again, be a sport and tie FLT to V_{CC} through a 1k resistor.

Intel's and AMD's 188/186 processors let you tristate the entire device by overdriving one or more output pins to ground during reset. Good news: Because these are CPU outputs, your circuit cannot drive the pins. You need no provision for debugging—with one exception. If you'd like to be able to have an emulator reset the device under software control, be sure that it can overdrive RESET. Use an open-drain reset circuit, with appropriate pullup.

Embedded-hardware engineers can accidentally or maliciously design a system that will make software development an order of magnitude harder than it should be. Smart software gurus will bring donuts and coffee to their hardware partners' desks and listen attentively to extensive stories of the latest PLD battle. We can all learn from Ford's success with the Taurus by communicating frequently with our software counterparts.

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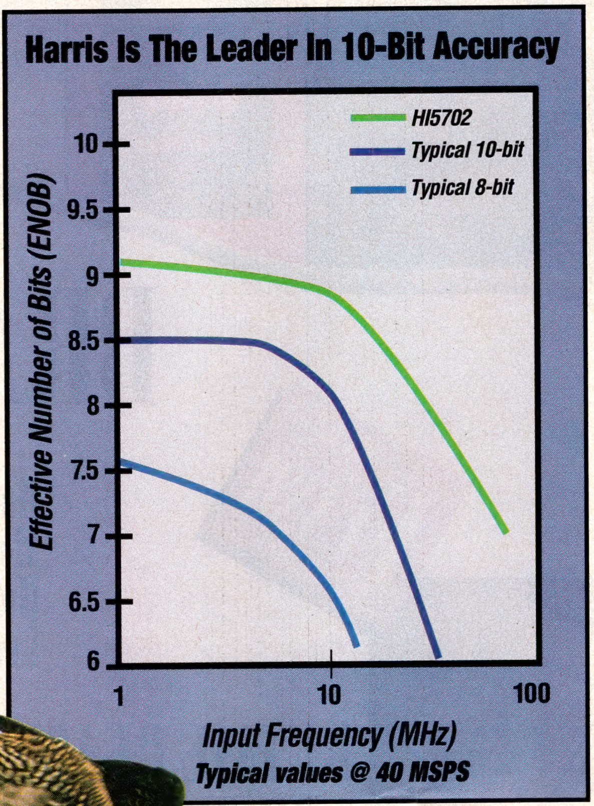

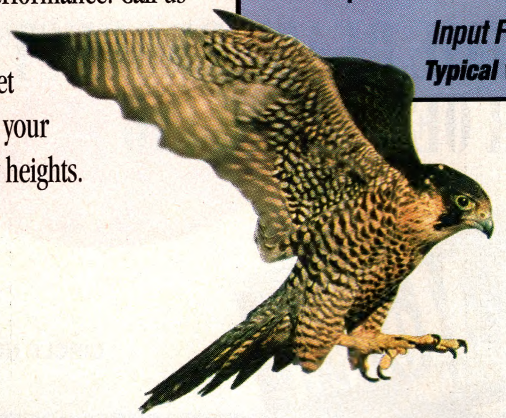

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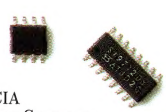

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